Switched-Beam 60 GHz Endfire Circular Patch Planar Array With Integrated 2-D Butler Matrix for Chip-to-Chip Space-Surface Wave Communications

by

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As members of the Dissertation Committee, we certify that we have read the dissertation prepared by Prabhat Baniya, titled Switched-Beam 60 GHz Endfire Circular Patch Planar Array With Integrated 2-D Butler Matrix for Chip-to-Chip Space-Surface Wave Communications and recommend that it be accepted as fulfilling the requirement for the Degree of Doctor of Philosophy.

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Final approval and acceptance of this is contingent upon the candidate's submission of the final copies of the dissertation to the Graduate College.

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Dedication

To my niece Arshiya

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Abstract

The complexity of chip interconnection on a multicore multichip (MCMC) module using the traditional wired interconnects increases with the chip count. The global wired interconnects that run across the entire module must be made longer as more chips are placed on a larger module. Since the interconnect delay grows as the square of the interconnect length, the global wired interconnects can become a major bottleneck of the computing performance in such systems.

This dissertation presents a new type of hybrid space-surface wave interconnect (HSSW-I) using 60 GHz switched-beam antenna arrays to provide high-speed communication between the chips. The antennas communicate at near the speed of light through radiation in the air above the chips and through surface waves at the air-dielectric interface, and thus avoid lengthy delays. Each array consists of four center-fed circular patch elements with side vias in a 2×2 planar grid arrangement. The arrays enable multi-gigabits-per-second (Gbps) reconfigurable interchip communication when integrated with the proper chip transceivers. The main beam of the array is switched in the horizontal plane containing the chips, by changing the interelement phase shifts. The switching of the main beam is analyzed and verified through full-wave simulation. A compact two-dimensional (2-D) Butler matrix feed network is designed, implemented, and integrated with the circular patch planar array. The matrix is a four-input, four-output, i.e., 4×4 network consisting of four interconnected quadrature (90°) hybrid couplers and allows endfire scanning of the array main beam along the four diagonal directions in the horizontal plane. The realized antenna module is a thin multilayer microstrip (MS) structure with a footprint small enough to fit over a typical multicore chip. The antenna module provides a seamless and practical way to achieve reconfigurable interchip communication in MCMC systems. A multiantenna module (MAM) consisting of five antenna modules

that emulates diagonal interchip communication in MCMC systems is fabricated. The simulation and measurement of the transmission coefficients between the antenna modules on the MAM are performed, and the signal-to-noise ratio (SNR) and signal-to-noise-plus-interference ratio (SNIR) of the links are calculated. A link decomposition simulation technique to determine the relative contribution of space and surface waves is also applied. A transmission link model is devised based on the leaky wave effect shown by the antenna arrays and the model coefficients are determined from the simulation data. The link model is then extrapolated at various distances and compared with more measurement and simulation results for verification. Finally, realistic link budget calculations are performed based on the measured and simulated data. The calculations show that the antenna modules using the HSSW-I can achieve raw data transfer rates up to 42.24 Gbps at 20 mm distance with low bit error rates (BERs) in the absence of interference, when used with the state-of-the-art 60 GHz complementary metal oxide semiconductor (CMOS) transceivers.

Chapter 1
Introduction

1.1 Background

The advances in complementary metal oxide semiconductor (CMOS) device fabrication have resulted in transistors with minimum feature size, such as the minimum channel length L_c between the drain and the source of a transistor, as depicted in Figure 1.1 [1], in the tens of nanometer (nm).

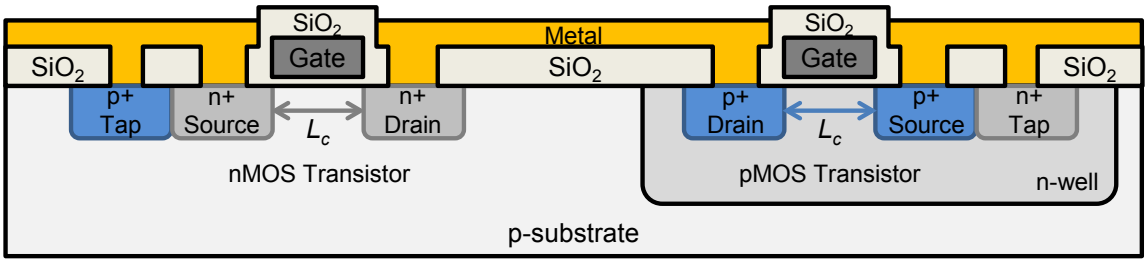


Figure 1.1. Cross-section of a basic inverter implemented in CMOS technology with nMOS/pMOS transistors, silicon dioxide (SiO_2) insulator, polysilicon gates, and metal contacts. (Source: N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective.* 4th Edition. Copyright © 2011, Pearson Education, Inc. Reprinted by permission of Pearson Education, Inc., New York, New York.).

The smaller transistors, which also switch faster because of their smaller size, can be packed more densely, in several billions, onto an integrated circuit (IC) chip to create faster microprocessors [2]. The increased clock frequency of such a vast number of transistors, however, results in increased overall power dissipation causing thermal stress and raising reliability issues. To keep the power consumption in check, the clock frequencies of the microprocessors have been capped [1, 2]. In the conventional CMOS digital circuits [3], there are three main contributors to the total average power consumption (P_{total}). They are switching power consumption (P_{switch}), short-circuit

power consumption (P_{sc}) and leakage power consumption (P_{lk}), as captured in the following equation:

$$P_{total} = P_{switch} + P_{sc} + P_{lk} \tag{1.1}$$

P_{switch} is associated with the charging and discharging of transistor load capacitances in the CMOS logic gates of ICs during each clock cycle [4]. It increases significantly as the chip size and integration density is increased. P_{switch} is dependent on several key parameters as given by

$$P_{switch} = \alpha f_{clk} C_{load} {V_{DD}}^2 \tag{1.2}$$

where α is the activity factor, f_{clk} is the clock frequency, C_{load} is the total load capacitance and V_{DD} is the supply voltage at the transistor drain.

The activity factor α takes into consideration that a logic gate may not undergo switching every clock cycle. The capacitance C_{load} represents the total output (load) capacitance, dominated mostly by the input capacitances of the transistor gates and the parasitic capacitance associated with the interconnection lines. As the transistor density on the chips is increased, the individual transistors can operate at much higher clock frequency which means more switching events can take place per second. This also means faster computation times are possible but at the cost of higher power dissipation. P_{switch} increases linearly with the clock frequency [4]. P_{sc} is due to the finite rise and fall times of the transition signals, which establish momentary direct path between the power supply and ground. P_{lk} is the result of the leakage mechanisms associated with the reverse bias that is inherent in the doped semiconductor even when the transistors are not switching. P_{sc} and P_{lk} are not a strong function of the chip density and size.

Chip manufacturers have found a way around the issue of higher switching power consumption associated with the increased clock frequency, by taking advantage of parallel processing. Such processing systems use multiple processing units called

cores, on a single chip to increase the computational performance and are appropriately called chip multiprocessors (CMPs). The clock frequencies of the cores are capped to avoid increasing the switching power. Computer programs are written to breakdown a large computational problem into smaller ones that are solved by the cores simultaneously, so as to realize the performance improvement offered by such hardware. Moore's law thus holds roughly to this day, as the total transistor count continues to double approximately every 18 months, albeit on a larger chip with multiple cores [1].

Although the decrease in feature size has significantly reduced the intrinsic transistor switching delays, the interconnect delays (especially associated with long wires on a chip) have not scaled down with feature size. This trend has caused the wired interconnects to be a bottleneck in the system performance.

1.2 Chip Interconnects

Chip interconnects can be broadly categorized into local, semiglobal and global types based on the length of the connection [1]. Local interconnects establish connection between smaller units such as the transistors and gates on a chip and become shorter as technology scales. Semiglobal interconnects run between larger blocks such as between cores of a CMP and also scale down with technology. Global interconnects run across an entire chip, such as for intercore bus connections and clock distribution. They can also run between chips in a multichip module (MCM). The global interconnects have the longest line lengths and the highest delays. The overall chip size and complexity have been steadily increasing to accommodate more cores. As a result, the average length and delay of the global interconnection lines have been growing as well and it can take multiple clock cycles for signals to traverse the chip. The interconnect delay τ grows as the square of the interconnect length L [5], expressed

as

$$\tau = RC = rcL^2 \tag{1.3}$$

where r is the resistance per unit length, c is the capacitance per unit length, $R = rL$ is the interconnect resistance, and $C = cL$ is the interconnect capacitance.

Repeaters (e.g., inverters) can be used with semiglobal and global interconnects to reduce the delays. By optimally placing repeaters along the long lines, the delay can be made linear with the length. Longer lines consume more power due to the higher resistance and capacitance associated with them. The interconnecting wires have been getting narrower, and the spacing between the wires has been decreasing to accommodate the increasing integration density. As a result, interconnect resistance has been going up causing increased power dissipation. Simultaneously, capacitive coupling between neighboring lines, known as, crosstalk, has been increasing resulting in increased coupling noise [5].

The global interconnects become the most problematic, as the feature size gets smaller with each CMOS process generation. This is because the global delays (even with optimal repeaters incorporated) decrease at a slower rate than the transistor delays, as shown in Figure 1.2 [5]. Although the repeater delays scale down with faster transistors, the global delays do not scale down at the same rate due to the global lines getting longer each generation to accommodate the increased chip size [5].

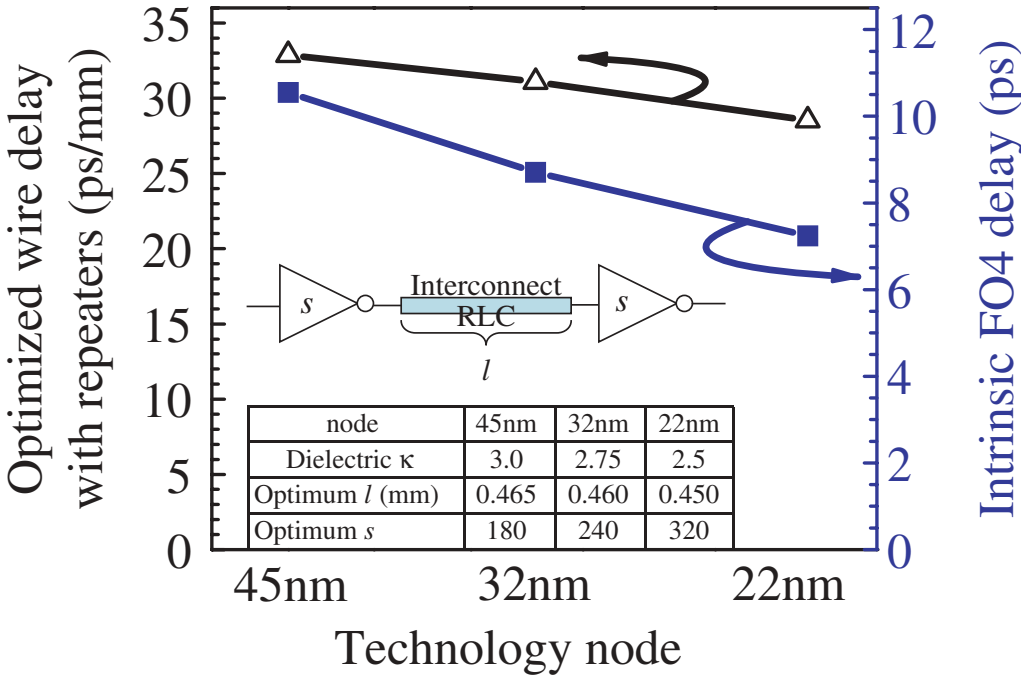


Figure 1.2. Delay improvement of three CMOS process generations for the transistor with the fanout-of-4 (FO4) load and the global interconnect with optimal repeaters. (Source: J. N. Burghartz, Ed., *Guide to State-of-the-Art Electron Devices.* Copyright © 2013, John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.).

CMOS processes have several metal, either copper (Cu) or aluminum (Al), layers of interconnect. Each layer is separated from the other by either SiO_2 or low dielectric constant (low-k) material to reduce capacitance, as shown in Figure 1.3. The transistors sit at the bottom with a progressively wider and thicker stack of metal layers on top [1]. The topmost metal layer offers the least resistance and thus has been conventionally used for providing fast input/output (I/O) global interconnections through solder bumps, pins or pads, as illustrated in Figure 1.3 [6]. The top layers have wider pitch to accommodate wider wires and they can sometimes limit the I/O pad count, which could be problematic for chips with large numbers of I/O.

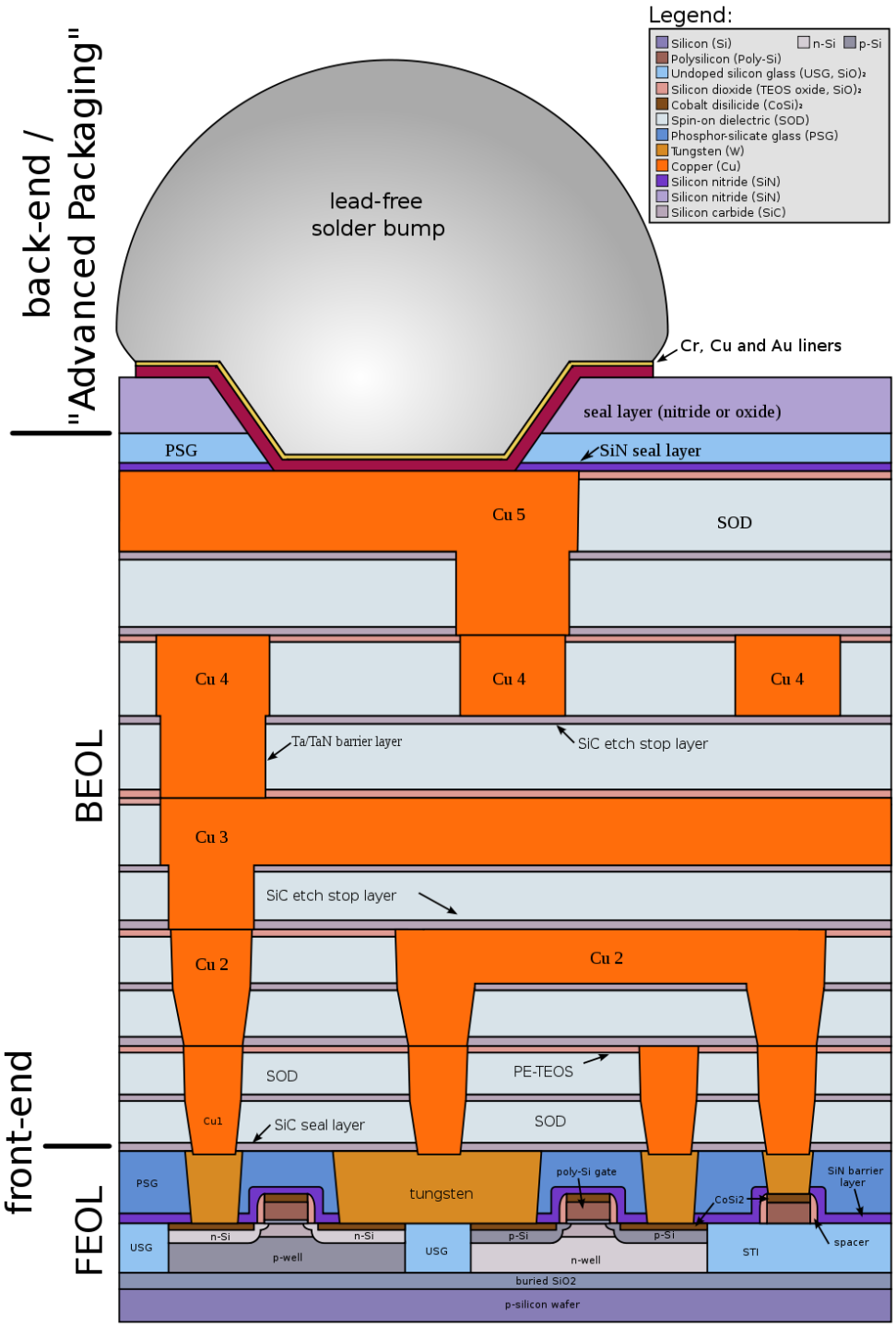


Figure 1.3. Schematic of metal interconnect layers with solder bump in a CMOS process [6].

The resistance per unit length r, given the dimensions of a wire as depicted in Figure 1.4 [1], can be calculated as follows [5]:

$$r = \frac{R}{L} = \frac{\rho}{tw} \tag{1.4}$$

where ρ is the resistivity, w is the width, and t is the thickness of the metal (Cu or Al).

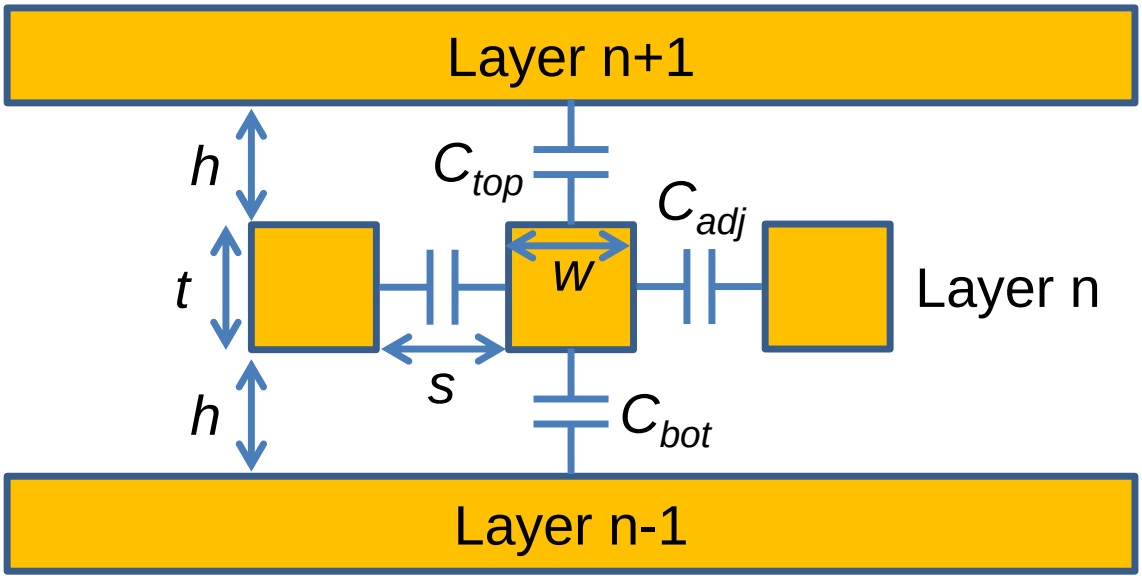


Figure 1.4. Multilayer wired interconnect. (Source: N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective.* 4th Edition. Copyright © 2011, Pearson Education, Inc. Reprinted by permission of Pearson Education, Inc., New York, New York.).

On the other hand, the capacitive interactions between closely spaced wires on and between the layers can be quite complex to estimate [1]. An upper bound on the total capacitance of a wire, assuming the layers above and below are solid ground planes (true when the layers are not switching), is given by the multilayer capacitance model depicted in Figure 1.4. The total capacitance C of a wire is the sum of the capacitance to the adjacent neighbors C_{adj} on the same layer, to the layer above C_{top},

and the layer below C_{bot}, as expressed in the following equation [1]:

$$\begin{aligned} C &= 2C_{adj} + C_{top} + C_{bot} \\ &= \epsilon_0 L \left(2\epsilon_{ox} \frac{t}{s} + 2\epsilon_{ox} \frac{w}{h} \right) + C_{fringe} \end{aligned} \tag{1.5}$$

where ϵ_{ox} is the dielectric constant of SiO_2 or low-k dielectric, and C_{fringe} is the fringing capacitance associated with fringing fields at the edges of the wire. C_{fringe} must be numerically solved to get accurate estimates. In reality, since the layers above and below are not solid planes, C_{fringe} must be interpolated based on the density of the metal wires on those layers. The interpolation accuracy can be limited, especially if the wire density is not well known, making the estimation of C_{fringe} hard and complicated. From (1.5), the capacitance per unit length can be calculated as follows:

$$c = \frac{C}{L} = \epsilon_0 \left(2\epsilon_{ox} \frac{t}{s} + 2\epsilon_{ox} \frac{w}{h} \right) + \frac{C_{fringe}}{L} \tag{1.6}$$

Thus, the metal-dielectric (wired) interconnects have inherently higher delays and latency than the free-space transmission because of the capacitive effects between the metal layers.

1.3 System-on-Chip (SoC)

CMPs must have low latency and high throughput interconnection between cores to be computationally efficient. CMPs are therefore based on a SoC integrated system that combines different functional components: cores, cache memory (L2 and L3), controllers, I/O links, interconnects, timers, interfaces, etc., on a single die/chip, as illustrated in Figure 1.5, to realize an efficient and compact computing unit.

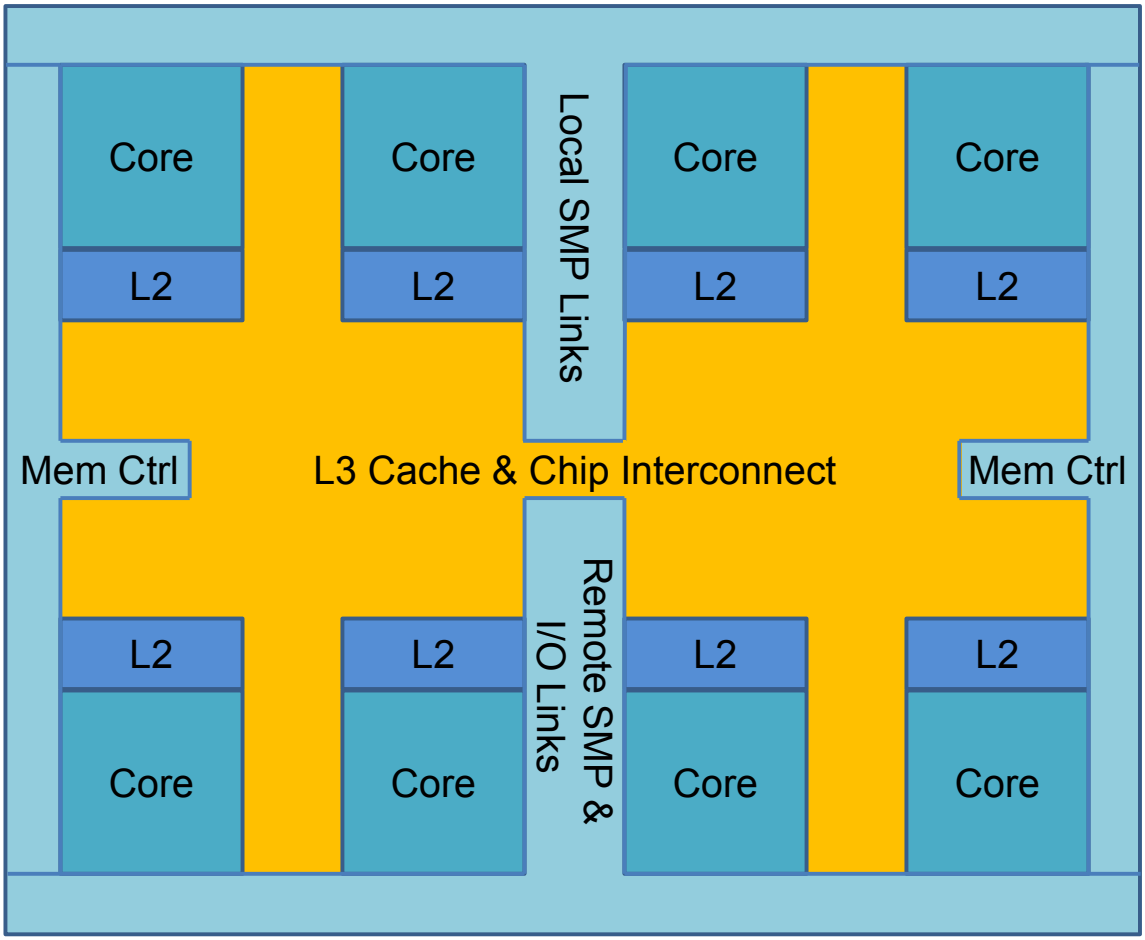


Figure 1.5. An illustration of eight-core symmetric multiprocessing (SMP) chip with different SoC components, based on IBM's POWER7 CPU [7].

The power consumption in the interconnection lines, further limits how many cores can be placed on a single chip and be effectively utilized at the same time. Furthermore, the complexity of such systems dramatically increases as they are scaled up to include more cores. In massively multicore processors, with tens to hundreds of cores, a fully reliable deterministic system is difficult to achieve because of the increasing involved interactions between ever increasing components [8]. On-chip global interconnects cannot be modeled as a predictable delay channel due to the undesirable and hard-to-estimate parasitics associated with the closely spaced lines. Data errors can occur due to the increase in electrical noise and functionally correct

operation of the system may not always be achieved every time an instruction is executed. Furthermore, global coordination using a single clock source is hard to achieve and can limit the performance. Therefore, such systems will benefit from using different clocks, becoming a distributed SoC that is globally asynchronous but locally synchronous. However, the synchronization errors cannot be avoided due to the use of multiple clocks [8].

1.4 Network-on-Chip (NoC) and MCM

Instead of relying solely on deterministic logic models, the NoC paradigm treats the SoC as a micro-network of components and provides a complete abstraction of on-chip physical interconnect lines for the network stack layers above, similar to the abstraction of physical wires in general computer networking [8]. The NoC enabled SoCs rely on network control protocols to maintain quality of service on the on-chip links and also relax the design of physical interconnections, to some extent. The NoC concept has also been extended to connect several SoCs to form an even larger computing unit called the MCM, as illustrated in Figure 1.6. The MCM shown has four dual-core SoC dies that are integrated onto a base substrate with wired interconnects, as illustrated in Figure 1.7 for a pair of chips. The wired interconnects are the transmission lines which can take the form of stripline, microstrip (MS) line or coplanar waveguide (CPW) [9] in the MCM substrate.

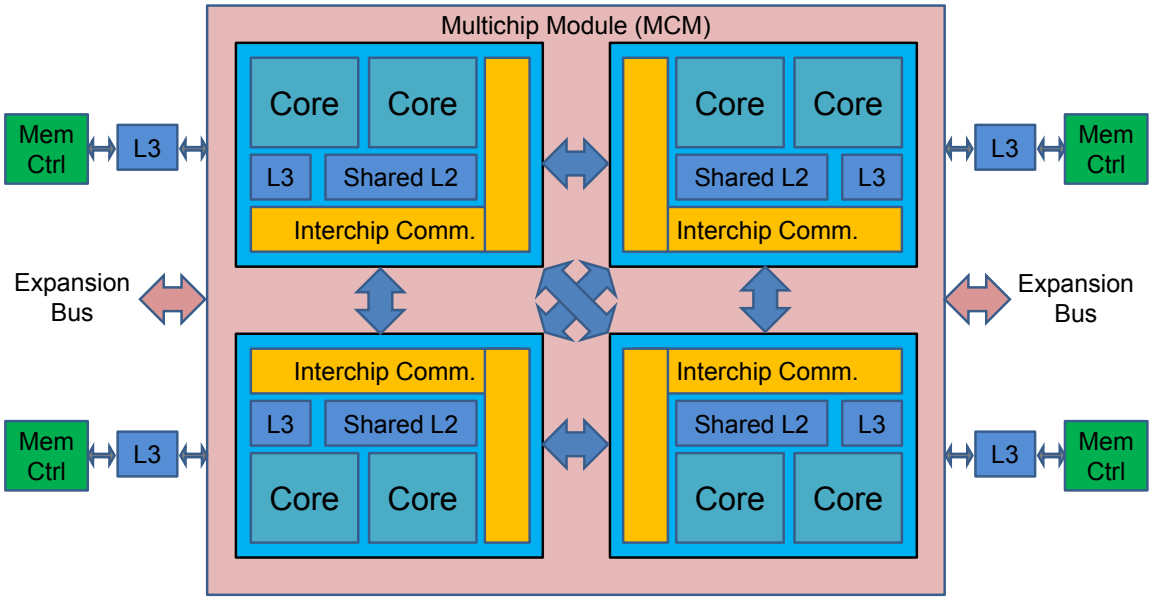


Figure 1.6. MCM with four dual-core dies and wired chip-to-chip connections. The expansion buses increase scalability [7].

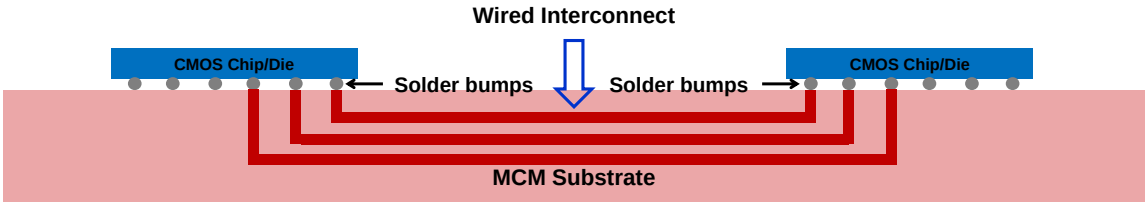


Figure 1.7. Wired interconnects connecting two CMOS chips/dies in the MCM substrate [9].

1.5 Interconnect Technology Comparison

As previously discussed in Section 1.2, the conventional wired interconnects can be a major bottleneck, especially in the MCM systems. Several interconnects, alternative to the conventional metal-dielectric interconnect, have been investigated by the researchers for global interconnection. These include three-dimensional (3-D) integrated circuit (IC) [1, 10], optical, radio frequency interconnect (RF-I), millimeter-wave (mmW) wireless interconnect, and surface wave interconnect (SW-I) [11]. They

are not meant to completely replace the conventional wire, but rather supplement them by providing high-speed connections between distant components in a module.

Each interconnect technology offers unique benefits but with added complexity, area, and power consumption overhead. Their merits and demerits are aptly summarized in Appendix A [11]. A high-level comparison of the key features of these technologies is given in Table 1.1 for convenience.

Table 1.1. Comparison summary of interconnect technologies

Features	**Wire**	**3-D IC**	**Optical**	**RF-I**	**mmW**	**SW-I**
Integrability	High	Medium	Low	Medium	Medium	Medium
Delay	High	Medium	Low	Low	Low	Low
Bandwidth (BW)	Low	Medium	High	High	High	High
Power Decay	Medium	Medium	Low	Low	High	Medium
Complexity	Low	Medium	High	Medium	Medium	High
Scalability	Low	Medium	Medium	Medium	High	High
Noise	Medium	Medium	Low	Medium	High	Medium
Cost	Low	Medium	High	High	Low	Medium
Area	Low	Low	High	Medium	Medium	Medium

1.6 Proposed Multicore Multichip (MCMC) Architecture

The traditional wired interconnects have to be made longer as more and more chips are placed on a larger module [11]. Consequently, the increased interconnect delay, power consumption, and wiring complexity limit the number of chips that can be placed on a module. One way to circumvent this limitation is to extend the NoC and MCM paradigm to connect several multicore SoC chips/dies with antennas to form an even larger multiprocessing unit. The NoC techniques are used to provide interchip communication in addition to intercore communication, and thus realize a MCMC computing unit [12]. Figure 1.8 illustrates a MCMC unit with nine chips in a 3×3 arrangement, each chip with multiple cores [13]. The cores on a chip communicate through the short on-chip and high-speed wired links. The long distance

in-plane communication between chips is done via the pattern switchable mmW antenna arrays, eliminating power consuming, complex, and long wired connections, and improving scalability. Furthermore, having the reconfigurable pattern allows the antenna arrays/chips to dynamically communicate to their surrounding neighbors.

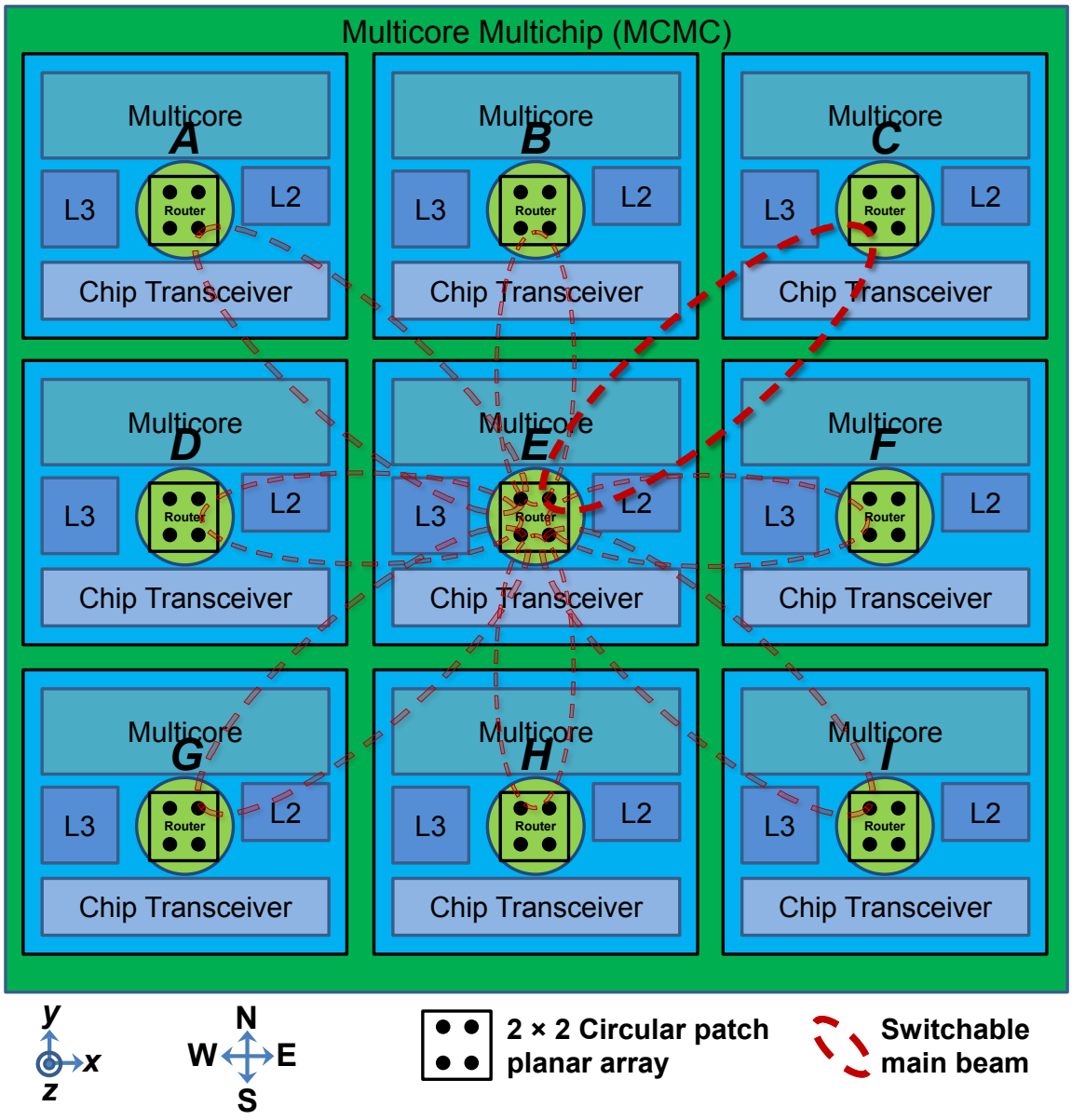


Figure 1.8. 3 × 3 MCMC architecture with chip-to-chip communication using pattern switchable mmW antenna arrays [13].

This scalable architecture can realize a high-performance computing (HPC) system through massive parallel processing since it provides a way to readily incorporate and efficiently link hundreds of cores together. Such computing modules would offer performance needed to solve demanding computing problems. This massive level of integration of multicore chips in a module is necessary in computationally intensive applications such as weather forecasting, mineral exploration, molecular dynamics, and human brain mapping. The push for fast computation is thus enormous. The multicore chips communicate with one another via the global interconnect fabric formed from the antennas. Since there is a frequent transfer of data and information between the chips, the computational speed can be limited by the communication speed between the chips. Thus, the technology and topology of global interconnect plays a significant role in the network and computational performance of massively multicore systems such as the MCMC. The most commonly used interconnect topologies are briefly discussed in Appendix A. The use of inherently wide BW mmW antenna arrays will ensure high throughput communication between the chips.

1.7 Proposed Hybrid Space-Surface Wave Interconnect (HSSW-I) With 60 GHz Switched-Beam Antenna Arrays

In this dissertation, switched-beam circular patch planar arrays are used to provide reconfigurable chip-to-chip communication at 60 GHz, as illustrated in Figure 1.8. These arrays are fabricated on a separate low-loss antenna substrate and designed to be packaged on top of the chips by connecting them to the integrated chip transceivers with solder balls [14], as shown in Figure 1.9. The substrate acts as a hybrid space-surface wave interconnect (HSSW-I) where both space and surface wave coupling occurs and in-plane communication takes place. The antennas communicate through radiation in the air above the substrate as well as through the surface waves at the air-substrate interface, both at near the speed of light c_0 [11] with the lowest

latency possible (due to negligible resistive/capacitive effects as opposed to wires). For example, the delay associated with the HSSW-I is about 3.3 ps per mm [$\tau = 1/(1000c_0)$] of the interconnect length whereas the global wired interconnect in the 22 nm CMOS process has about 29 ps per mm of the interconnect length (see Figure 1.2). The HSSW-I also offers the cost-effective and low design complexity of mmW wireless interconnect while providing the lower power decay of SW-I. Although the path loss due to spreading is inherent in the hybrid links, the nearly lossless air above the substrate and the low-loss substrate contribute little to power dissipation and heating within the module.

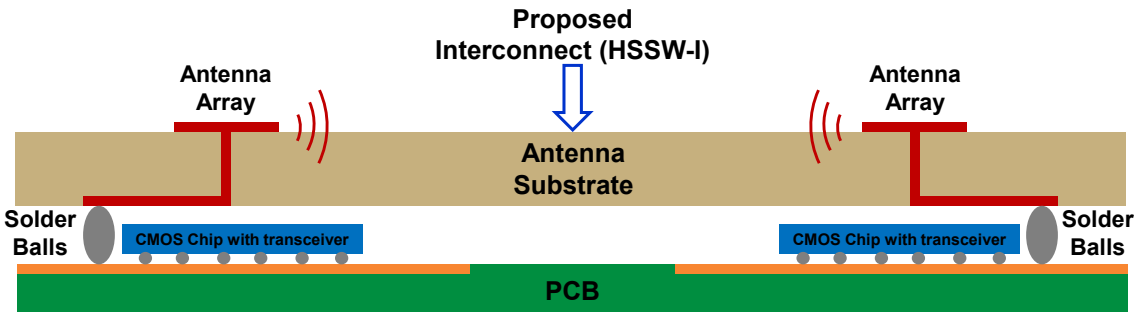


Figure 1.9. Proposed HSSW-I for chip-to-chip communication in MCMC architecture.

The antenna arrays are designed for 60 GHz operation so that they can be easily integrated with the existing CMOS transceivers compliant with the Institute of Electrical and Electronics Engineers (IEEE) 802.11ad and 802.11ay standards. Both standards allow unlicensed frequency operation around 60 GHz with a broad BW of 2.16 GHz and high throughput of up to 7 gigabits-per-second (Gbps) per channel [15]. A 60 GHz HSSW-I link based on the standard can provide multi-Gbps data rate needed for interchip communication, with the proper design of the transceiver [16] and antenna components [17]. Even higher throughput is achievable with multichannel operation using the newer IEEE 802.11ay standard [18]. A low latency interconnect such as the HSSW-I with broad BW will ensure that the actual throughput is high.

Figure 1.8 shows the switched-beam array, a four-element circular patch array

in a 2 × 2 grid arrangement, over the chip routers. The arrays can be thought of as the hub of interchip communication. Specifically, the hybrid links using the switched-beam antenna arrays between adjacent routers in the diagonal directions, namely *E–A*, *E–C*, *E–G*, and *E–I*, are considered. Because of the non-wired topology of HSSW-I, single hop communication in the diagonal directions is made possible, improving the communication and computational speed [19]. A mesh topology wired connection between the chips (where each chip is only wired to its north, south, east, and west neighbors) would require two hops to communicate in the diagonal directions. Thus, the addition of the proposed interconnects in the diagonal directions to the traditional mesh connection can significantly improve the interchip communication. Network simulations in [19] have shown reduction in packet latency, increase in system throughput, and decrease in total energy consumption when wireless interconnects in the diagonal directions are augmented to the wired mesh connection, which is referred to as the hybrid NoC (HyNoC) topology. Even higher performance improvements can be expected if the wireless interconnects in the HyNoC topology are replaced with the proposed interconnects.

The antenna arrays can also provide real time reconfiguration of the data paths as broken links can be bypassed by switching the array main beam. In addition to broad BW and switchable main beam, the 60 GHz antennas for interchip communication have other challenging requirements. These include CMOS connectivity, small footprint, and low power dissipation. The design of the antenna arrays thus requires a careful and thorough consideration.

1.8 Millimeter-Wave Propagation Characteristics

The mmW electromagnetic spectrum ranges from 30 GHz to 300 GHz, corresponding to the free-space wavelength λ_0 from 10 mm to 1 mm. An advantage of using higher carrier frequency is wider available BW [20]. For line-of-sight (LoS) propagation, the

free-space path loss is inversely proportional to λ_0^2 [21]. The mmW links experience high free-space spreading loss due to their relatively smaller wavelengths and therefore, the communication distance is limited. In addition to the spreading loss, the total path loss is also affected by atmospheric absorption due to molecular oxygen (O_2) and water vapor molecules (H_2O) at certain frequencies in mmW spectrum, as shown in Figure 1.10 [22, 23]. The mechanical resonance of O_2 is responsible for attenuation peak near 60 GHz. The O_2 absorption around 60 GHz is about 15 dB per kilometer. Typical interchip distances in MCMC systems can range from few to several tens of millimeters, depending on the size of the chips used [13, 14]. Hence, the atmospheric absorption is not expected to have any major effect on the link performance at these distances. Nevertheless, it can be helpful in reducing interference between the mmW systems at long range, if the links are also operated at the 60 GHz carrier frequency. For these reasons, the proposed antenna arrays will be designed to operate at around 60 GHz.

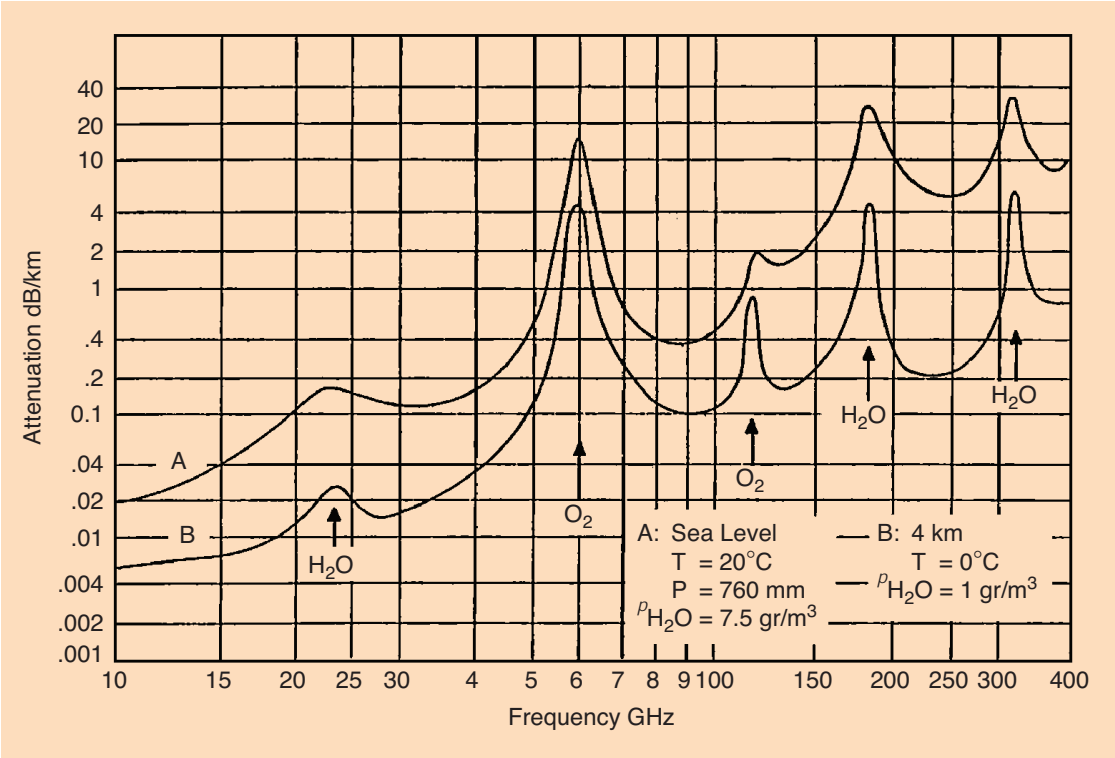


Figure 1.10. Atmospheric attenuation (dB/km) of mmW spectrum due to the molecular oxygen (O_2) and water vapor (H_2O) [22].

1.9 Antenna Metrics

1.9.1 Transmission, Gain, and Impedance BWs

The antennas play a significant role in determining the BW of wireless and hybrid links. The *transmission BW* of a channel can be defined as the frequency range over which the signal-to-noise ratio (SNR) is maintained within 3-dB of the peak value. If channel noise is constant over the frequency range, then the transmission BW is simply the 3-dB transmission coefficient ($|S_{21}|$) BW, as depicted in Figure 1.11(a). For the LoS wireless communication in the far-field, the transmission of signal from transmitter (TX) antenna to receiver (RX) antenna is given by the Friis equation as

follows [21]:

$$\frac{P_r}{P_t} = |S_{21}|^2 = \left(1 - |S_{11}|^2\right)\left(1 - |S_{22}|^2\right)\left(\frac{\lambda_0}{4\pi R}\right)^2 G_{TX} G_{RX} \tag{1.7}$$

where P_r and P_t are the received and transmitted powers respectively, R is the distance between the antennas, λ_0 is the free-space wavelength, S_{11} and S_{22} represent the reflection coefficients of the TX and RX antennas, respectively, and G_{TX} and G_{RX} represent the gains along the LoS of the TX and RX antennas, respectively.

Equation (1.7) provides valuable insight into the transmission (S_{21}) BW of a wireless link which is a function of the path loss, and the reflection coefficient and gain of the antenna. The *gain BW* of an antenna is defined as the frequency range where the reduction in gain is within 3-dB of the value at the center frequency, as depicted in Figure 1.11(b). The transmission BW depends on both the impedance and gain BWs. The gain BW dominates impedance BW in (1.7), and therefore, the former is much more important to consider.

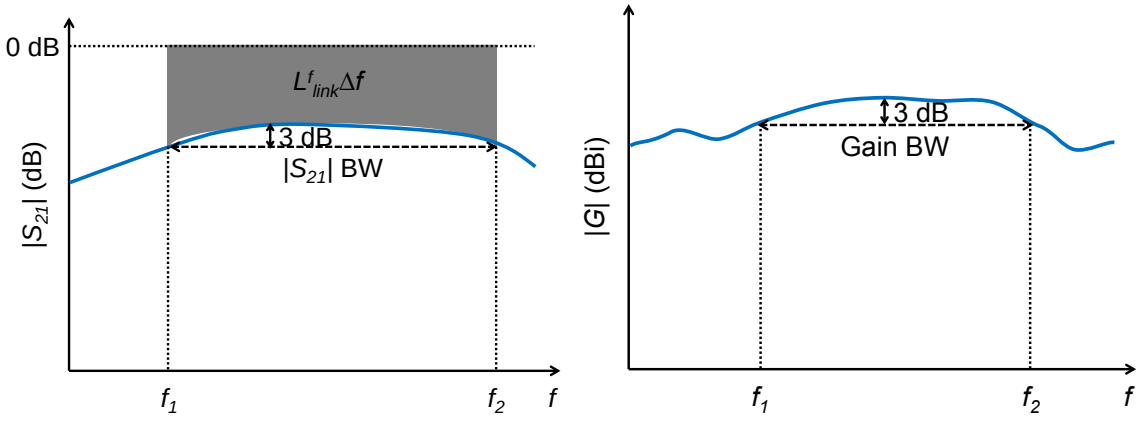


Figure 1.11. (a) Transmission BW of a link. (b) Gain BW of an antenna.

A good antenna design, nonetheless, should consider both, as their interplay determines the transmission BW. Using the 3-dB criterion for the transmission BW imposes a stricter 1.5-dB criterion on the gain BW (at each end of the link) which

can be derived from (1.7), assuming reflection coefficient is constant over the band and identical TX/RX antennas and LoS gains i.e., $|S_{11}| = |S_{22}|$ = constant and $G_{TX} = G_{RX}$, respectively. However, the impedance BW is relaxed to a $|S_{11}| \leq 5.3$ dB criterion at each end of the link, instead of the usual 10-dB criterion, to maintain the 3-dB transmission BW provided the gain is constant over the band. It is important to note that for the chip-to-chip communications considered, the far-field criterion may not strictly hold because of the small distances between the chips. Therefore, the dependence of $|S_{21}|$ on the reflection coefficient and gain is not straightforward like in (1.7) due to the near-field effects. The transmission BW is a better overall figure-of-merit since the gain BW is only applicable in the far-field. In this dissertation, a new link model is introduced to capture the $|S_{21}|$ behavior of the HSSW-I involving the proposed arrays, and the link budget calculations are performed based on the $|S_{21}|$ of the link.

1.9.2 Antenna Noise Figure (NF)

Besides the BW, the NF of an antenna is another important metric that is useful for performance comparisons [24]. A low NF antenna, because of low intrinsic losses and thermal noise can provide higher SNR and channel capacity. High gain antennas with low-loss feed networks are therefore desirable. At the temperature $T = 290$ K, the NF is equal to the loss factor L_a [24], and is related to the radiation efficiency e_r as

$$\text{NF} = L_a = \frac{1}{e_r} \tag{1.8}$$

Equation (1.7) takes the signal loss due to e_r into account since gain G is related to e_r [21], expressed as

$$G = e_r D \tag{1.9}$$

where D is the directivity of the antenna. The intrinsic conductor and dielectric losses reduce the e_r of the antennas [21] and increase its NF. The internally generated

thermal noise increases with the physical temperature T_p of the antenna, and subsequently, the overall system noise is increased [24]. It is therefore important to also take into account e_r for noise calculations. The thermal noise generated as well as the background noise picked up by the antenna are considered for SNR calculations in this dissertation.

1.9.3 Link Loss

The transmission ratio in (1.7) dictates the amount of gain required for the low noise amplifier (LNA) in RX circuits for recovering some of the power lost in free-space transmission. Low path loss is desirable since low gain LNAs can be used to keep the power levels above RX's sensitivity and low gain power amplifiers (PAs) can be used at the TX. Amplifiers with lower gains have better noise performance. Moreover, transmission flatness over the band is another favorable characteristic since the gain required to recover the loss would also be flat, relaxing the requirement on the amplifiers used and reducing bit error rate (BER) in amplitude modulated schemes such as the quadrature amplitude modulation (QAM) [25]. The transmission ratio in (1.7), represents the free-space LoS link loss L_{link}, and can be expressed in dB as

$$L_{link}(\text{dB}) = -10\log_{10}\left[\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)\left(\frac{\lambda_0}{4\pi R}\right)^2 G_{TX}G_{RX}\right] \tag{1.10}$$

In general, when the far-field criterion does not hold, L_{link} can be calculated from the $|S_{21}|$ of the link as

$$L_{link}(\text{dB}) = -10\log_{10}|S_{21}|^2 \tag{1.11}$$

For convenience, L_{link} is usually defined for a certain R. In addition, L_{link} BW can also be defined using the 3-dB criterion around the center frequency and it is equal to the 3-dB transmission BW. L_{link} BW is thus another figure of merit useful for comparison purposes. The links that have lower L_{link} values over larger frequency range are desirable because they are more power efficient over a wider band [9].

Instead of calculating L_{link} at each frequency point, a metric, *link loss frequency budget* L^f_{link}, can be defined that takes into account the average link loss over a certain frequency range $\Delta f = f_2 - f_1$. It is calculated by integrating the transmission coefficient curve $|S_{21}(f)|$ over the frequency range as follows:

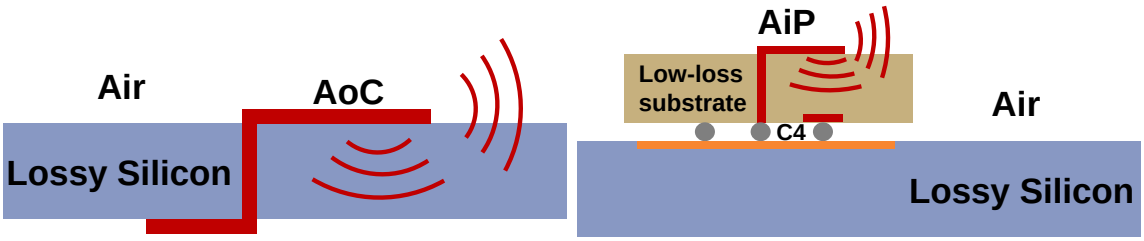
$$L^f_{link} = -10 \log_{10} \left(\frac{\int_{f_1}^{f_2} |S_{21}(f)|^2 df}{f_2 - f_1} \right) \quad \text{(dB)} \tag{1.12}$$

As depicted in Figure 1.11(a), (1.12) calculates an area that is proportional to the area between the 0 dB flatline (lossless transmission) and the $|S_{21}(f)|$ (dB) curve from f_1 to f_2, divided by the frequency range. The links with lower values of L^f_{link} are desirable since they have lower average loss within the specified band. L^f_{link} calculations are performed to determine the average SNR and signal-to-noise-plus-interference ratio (SNIR) of the HSSW-I link in this dissertation.

1.10 Antenna-on-Chip (AoC) and Antenna-in-Package (AiP) Solutions

The antennas for the traditional wireless interconnects can be broadly categorized into AoC and AiP solutions [26], as illustrated in Figure 1.12. In the AoC solutions, the antennas are integrated with the rest of the RF front-end circuits on a silicon-based chip such as the CMOS, as shown in Figure 1.12(a). However, due to the low resistivity of the silicon substrate, AoC implementations have low radiation efficiency [27] and thus gain. Although fabrication techniques exist to improve the AoC efficiency, the improvement is slight and not justified for the manufacturing complexity added. The AiP solutions generally offer high radiation efficiency because the antennas are fabricated on a low-loss substrate that is placed off the silicon chip but packaged with the chip through connections using bond wires or flip-chip (C4) bumps [28]. The C4

implementation is depicted in Figure 1.12(b). Such chip-to-package connections introduce inductive parasitics, which can limit the upper frequency bound of the front-end system. Compensation circuitry can be used to counter the effects of parasitics but at the expense of additional package area, which usually is not a problem for many applications [26]. The flip-chip technique exhibits wider BW and better performance than wire bonding because the parasitic inductance associated with short wide solder bumps is significantly less than the long thin wires [29]. Flip-chip connections also offer more rigidity than bond wire connections but are more susceptible to defect formation due to chip thermal expansion [26].



(a) (b)

Figure 1.12. (a) AoC. (b) AiP.

In this dissertation, an AiP implementation of the proposed arrays is pursued because of the higher radiation efficiency and the flexibility to design the antennas separately from the CMOS chips. The comparison of some of the fixed-beam 60 GHz AoC and AiP antennas, available in the literature, is summarized in Table 1.2 along with their performance metrics. The AiP antennas have higher peak gains and thus have lower L_{link}. Adding pattern reconfiguration capability to the proposed antennas will be a challenge due to the limited available area.

Table 1.2. Comparison of fixed-beam 60 GHz AoC and AiP antennas

Ref.	**Antenna Type**	**Peak Gain (dBi)**	**Gain BW (GHz)**	**$\|S_{11}\|$ BW (GHz)**	**e_r/ NF**	**Antenna Size (mm^3)**
[16]	Yagi-Uda (AiP)	7.1	10	20	–	$8.5 \times 4 \times 0.1$
[17]	Planar Aperture (AiP)	12.1	10	12.5	85% 0.7 dB	$12 \times 12 \times 1.1$
[27]	Yagi (AoC)	-10.6	–	10	10% 10 dB	-
[30]	Bondwire (AoC)	-1.4	14	3	50.9% 2.9 dB	-
[31]	Waveguide Aperture (AiP)	2.2	16	2.5	–	$6.4 \times 4.8 \times 1$
[32]	Patch Array (AiP)	16.6	–	12	–	$28 \times 28 \times 1.2$
[33]	Yagi (AiP)	6	–	2.3	93% 0.3 dB	$12.5 \times 8.6 \times 1.6$
[34]	Stacked Patch Array (AiP)	12.7	12	9	73.5% 1.3 dB	$20 \times 20 \times 0.8$
[35]	Slab Waveguide (AiP)	6	7	10.4	–	$8.4 \times 7.5 \times 1$
[36]	Yagi-Uda (AiP)	7.3	–	9	90% 0.5 dB	$5.7 \times 3.7 \times 0.9$
[37]	Patch Array (AiP)	18.2	7	4.7	–	$18.6 \times 18.6 \times 0.6$
[38]	Folded Dipole (AiP)	7	–	20	90% 0.5 dB	$4.2 \times 3 \times 0.8$
[39]	Slot Antenna Array (AiP)	15.4	9	13.9	90% 0.5 dB	$15 \times 5 \times 4.5$
[40]	Patch Antenna (AiP)	25.8	13.8	15	72% 1.4 dB	$32.6 \times 32.6 \times 3.5$
[41]	Patch AMC (AiP)	4	17.2	11	93% 0.3 dB	$9.5 \times 6.2 \times 0.6$
[42]	Patch AMC Array (AiP)	7	–	19	98% 0.1 dB	$6.2 \times 6.2 \times 0.6$

1.11 60 GHz CMOS Transceiver Circuits With Antennas

Researchers have shown the ability to create highly integrated CMOS transceivers for mmW short range wireless communication at 60 GHz. The 60 GHz carrier frequency offers much wider BW, which is important to realize the multi-Gbps data rate. This can pose challenging requirements such as high gain with flatness over wideband at both the transmitter and receiver ends. The 60 GHz transceivers have been implemented most popularly using either the dual-conversion or the direct-conversion architectures [25, 43]. Direct-conversion transceivers use only single stage of mixing avoiding the use of large intermediate frequency (IF) filters and are preferred for the on-chip applications because they are compact and consume less power. The basic architecture of a direct-conversion 60 GHz CMOS transceiver is shown in Figure 1.13 [20].

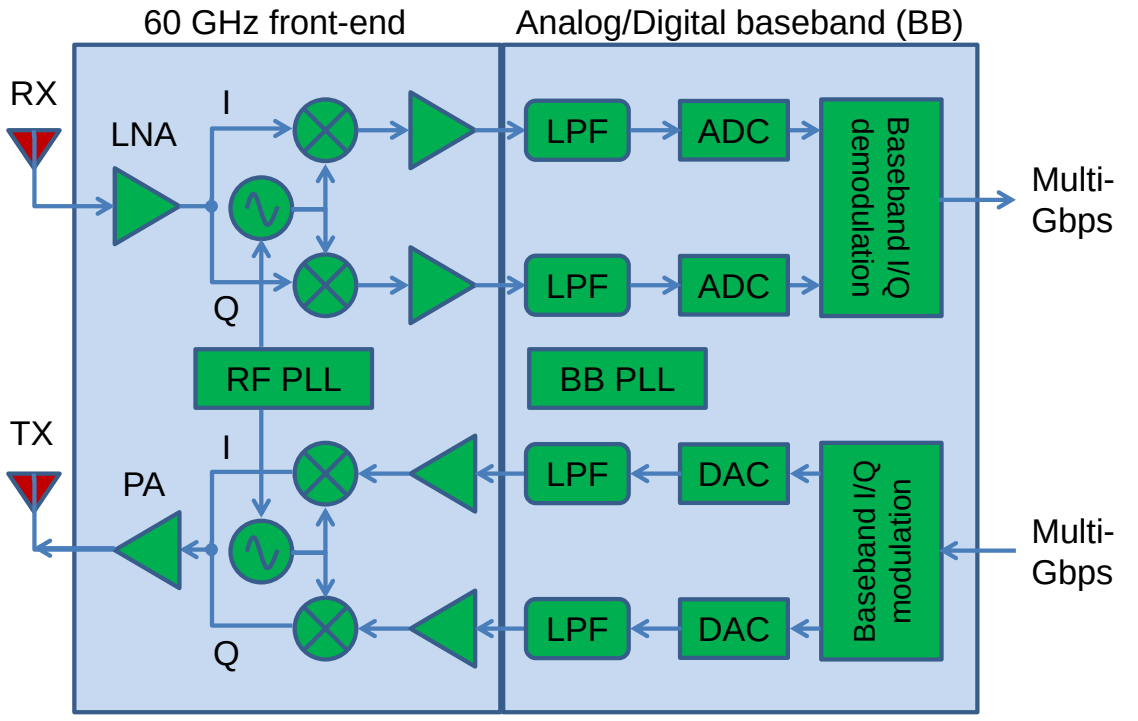


Figure 1.13. Basic components of a direct-conversion 60 GHz CMOS transceiver [20].

The channel BW of the transceiver is determined by the transmission BW associated with the cascaded blocks of RF components in the chain such as the amplifiers, mixers, oscillators, phase-locked loops (PLLs), low pass filters (LPFs), antennas, and the analog and digital baseband (BB) circuitry such as the analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The BW of each component must be much wider than the desired cascaded BW. This requires the design of wideband RF and BB components. Nonetheless, these components add very little area overhead on the chip [20]. The direct-conversion transceivers typically have performance issues arising from the in-band local oscillator (LO) phase noise and leakage, in-phase/quadrature (I/Q) mismatches and large LO frequency tuning range. The problems are particularly severe for the higher-order modulation formats. Dual-conversion transceivers perform better because the LO frequency and phase noise are considerably offset from the RF frequency, reducing the noise in the resulting IF signal. The LO operating frequency and tuning range are reduced as well. Also, I/Q modulation and demodulation can be performed at a much lower IF frequency, thus significantly reducing the I/Q mismatches. However, the dual-conversion transceivers use two stages of mixing, requiring the use of more components and relatively large IF filters [25]. They occupy more chip area and consume more power. Some of the highest reported throughput pertaining to 60 GHz CMOS transceivers with AiP implementation, available in the literature, are summarized in Table 1.3.

Table 1.3. Comparison of 60 GHz CMOS transceivers

Ref.	**CMOS Process**	**Data Rate (Mod.)**	**Antenna Type**	**Antenna Size (mm^3)**	**Peak Gain (dBi)**	**BER@ Distance**
[16]	90 nm	10.7 Gbps (OOK)	Yagi-Uda (AiP)	$8.5 \times 4 \times 0.13$	7.1	10^{-12}@ 10 cm
[18]	65 nm	42 Gbps (64-QAM)	Horn	–	14	10^{-3}@ 13 cm
[20]	65 nm	7 Gbps (16-QAM)	Waveguide MS (AiP)	$8.4 \times 7.5 \times 1$	6	–
[44]	40 nm	11 Gbps (ASK)	Bondwire Dipole (AiP)	–	0	10^{-11}@ 14 mm
[45]	40 nm LP	7 Gbps (16-QAM)	4×2 Patch Array (AiP)	–	7.5	–
[46]	65 nm	11 Gbps (16-QAM)	Waveguide Aperture (AiP)	$6.4 \times 4.8 \times 1$	2.2	10^{-3}@ 5 cm
[47]	45 nm SOI	5 Gbps (BPSK)	Slot Loop Antenna (AiP)	–	4.5	–

As shown in Table 1.3, it is possible to achieve multi-Gbps data rate required for interchip communication, using relatively small footprint antennas with low to moderate gains at 60 GHz. However, the antennas used in the works, given in Tables 1.2 and 1.3, have fixed beams and thus can only offer static links. They have limited practicality for use in the MCMC systems where switchable beams are required.

In this dissertation, the 60 GHz arrays are designed and built to realize the reconfigurable and non-wired links. These arrays are integrated with the proper feed networks and targeted for seamless connectivity with the existing 60 GHz CMOS transceivers to enable high throughput chip-to-chip communications.

1.12 The IEEE 802.11ad/ay Standard and Data Rates

The IEEE with the Wireless Gigabit Alliance (WiGig) has developed an industry standard *802.11ad* that allocates four channels, each with 2.16 GHz BW around the 60 GHz frequency, as shown in Figure 1.14 [15, 18, 48]. Moreover, the frequency band from 57.05 to 64 GHz, which is shared with the 802.11ad spectrum, is available for unlicensed usage in the United States (US) [15]. Unlicensed operation means there is no regulatory protection against power emissions from other devices over the frequency allocated and any communication devices operating in those bands have to be tolerant of interference generated by other potentially high powered devices. For example, there is a 60 GHz industrial, scientific, and medical (ISM) unlicensed band that spans from 61 to 61.5 GHz for purposes other than telecommunications [49]. It can interfere with the 60 GHz unlicensed band shared with the IEEE 802.11ad spectrum.

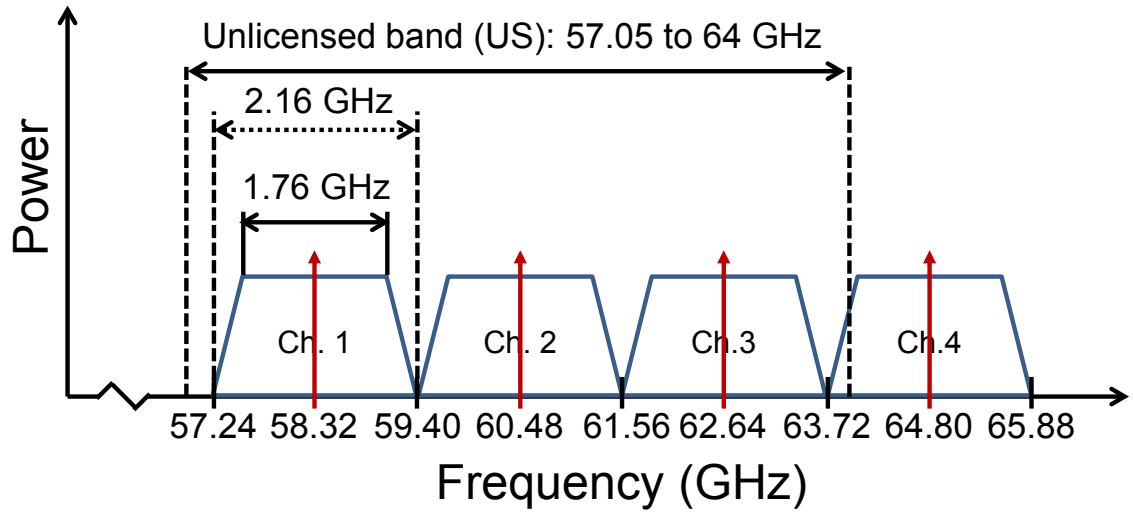


Figure 1.14. Spectrum allocations on the IEEE 802.11ad/WiGig standard [18].

Nonetheless, the atmospheric absorption peak near 60 GHz allows shorter frequency reuse distances because of higher interference suppression, which makes the 60 GHz unlicensed band in the IEEE 802.11ad standard especially attractive for short

range communications. The wide BW with the added benefit of unlicensed operation, makes multi-Gbps wireless communication appealing around the 60 GHz band. With unlicensed operation, higher transmitted power is allowed and subsequently, higher SNR can be attained on the wireless link. The transmitted power level limit is given in terms of effective isotropic radiated power (EIRP), which is 40 dBm for the unlicensed band in the US [50], as set by the Federal Communications Commission (FCC). Moreover, the IEEE 802.11ad/WiGig standard makes the 60 GHz band an excellent candidate for developing compliant CMOS transceivers. The specification in IEEE 802.11ad allows for up to 7 Gbps wireless raw data rates using 16-QAM modulation over a 2.16 GHz channel BW [15]. Out of the 2.16 GHz BW, 0.4 GHz is used as a guard band leaving 1.76 GHz of available BW [43, 51]. During modulation, if the binary bitstream with sharp transitions are used to modulate the carrier, it will result in a broad spectrum modulated signal around the carrier frequency. This can cause high adjacent channel interference. A baseband LPF must be used to shape the sharp bit transitions into a smoothly varying signal and thus limit the BW of modulated signal. Due to the slow roll-off of the practical filters, guard bands are required to minimize the adjacent channel interference.

To achieve the 7 Gbps data rate, the SNR must be high enough at the given distance to keep BER at acceptable levels. For the 16-QAM scheme, the number of bits in a symbol $N_b = 4$ and the maximum achievable data rate R_c is calculated using Hartley's law as [52]

$$R_c \leq N_b \times \text{BW} \tag{1.13}$$

Since the usable BW is 1.76 GHz, $R_c \leq 4 \times 1.76 = 7$ Gbps is achievable for each channel in the IEEE 802.11ad spectrum. Since SNR degrades (and BER increases) with increasing distance, the maximum rate can only be achieved at distances shorter than some specified maximum distance. Bonding all four channels, which is aimed in the successor standard IEEE 802.11ay, data rates up to 28 Gbps and 42 Gbps have

been achieved using the 16-QAM and 64-QAM schemes, respectively [18]. Coupled with higher order modulation support, data rates beyond 100 Gbps are being targeted with the IEEE 802.11ay standard. This would provide a good starting point for fast chip-to-chip communications in the MCMC systems. There are several factors that determine if the SNR required to establish a mmW link at any given data rate, can actually be achieved. These include the path loss characteristics, communication distance, allowed BER, modulation scheme, noise/interference sources, transceiver NF, implementation loss, and antenna gains [47].

The antenna arrays developed in this dissertation are aimed at providing sufficient gains with the added feature of reconfiguration so that a dynamic high throughput link can be established between the chips when properly integrated with the 60 GHz CMOS transceivers.

1.13 Dissertation Objectives and Unique Contributions

To summarize, the focus of this dissertation is the design and implementation of 60 GHz switched-beam antenna arrays with integrated feed networks to develop HSSW-Is for chip-to-chip reconfigurable communications. The main objectives of this dissertation are as follows:

- Design compact and low-profile switched-beam antenna arrays for pattern reconfiguration at 60 GHz.
- Design small footprint feed networks and integrate them with the antenna arrays.
- Develop the HSSW-I using the integrated antenna array modules emulating a realistic chip-to-chip communication scenario.
- Fabricate the antenna modules with the HSSW-I and simulate and measure the chip-to-chip signal transmission and interference.

- Devise a new link model that takes into account the power decay behavior of the HSSW-I and verify it with simulation and measurement.
- Analyze the link budget taking into account all the component losses, noise, and interference sources, and estimate the raw data rates achievable with the HSSW-I.

1.14 Dissertation Outline

This dissertation is organized into six chapters. Chapter 1 discussed the traditional wired interconnect and its associated limitations and introduced the HSSW-I for chip-to-chip communication in MCMC systems. Chapter 2 presents the detailed structure and simulation results of the 60-GHz switched-beam antenna arrays. Chapter 3 presents the design, implementation, and integration of the two-dimensional (2-D) Butler matrix feed network with the antenna arrays. Chapter 4 presents the realization of the HSSW-I using the antenna modules, and the simulation and measurement of chip-to-chip transmission coefficients between the antenna modules along with the link model and link budget calculations. Chapter 5 considers how certain manufacturing deviations can affect the performance of the antenna modules and the link. Finally, Chapter 6 concludes the dissertation with the summary of the important results obtained and potential future improvements.

Chapter 2
Switched-Beam 60 GHz Antenna Arrays

In this chapter, the proposed 60 GHz antenna array is designed and analyzed. Some of the contents of this chapter have been published in [13]. The array consists of four center-fed circular patch elements with side (shorting) vias in a 2 × 2 grid arrangement. The array is designed to have a small footprint so that it can fit on a typical multicore chip [53]. The array main beam is switched by changing the interelement phase shifts. The beam scanning is done in the horizontal chip plane to provide reconfigurable chip-to-chip communications. The switching of the main beam is analyzed and verified through full-wave simulation.

2.1 Introduction

In the MCMC architecture, since the antenna arrays all reside in the same azimuth plane (horizontal xy-plane in Figure 1.8), they must be capable of scanning their main beams in the lateral (endfire) directions to communicate with one another in the plane. This is different from pattern reconfiguration in mmW wireless local area networks (WLANs) and Wi-Fi networks where beam scanning is done mostly in the broadside, above the antenna plane [32, 54]. Therefore, the MCMC systems posit the unique requirement of 360° endfire scanning on the antenna arrays. The interconnects based on such arrays enable reconfigurable chip-to-chip communication in the horizontal plane. The 60 GHz antenna arrays surveyed in [55] only have broadside beam scanning capability. Recently, an endfire scanning array using magnetoelectric (ME) dipole elements has been demonstrated in [56] but the angular coverage is limited to 180°. A planar array of ME dipoles is presented in [57] but for 360° broadside scanning. The switched-beam antenna array presented in this dissertation has endfire scanning capability with 360° angular coverage.

2.2 Planar Array of Isotropic Elements

For the chip-to-chip communication scenario depicted in Figure 1.8, planar arrays are particularly well suited since they can provide a full 360° scan of the main beam [58]. This ensures that each chip is able to communicate with its adjacent neighbors in all eight directions: north, south, east, west, and the four diagonals, provided the array has enough elements to scan the main beam laterally in 45° steps, as shown in Figure 1.8. A linear array is not suited since it is not capable of achieving a 360° scan [58]. In this section, a planar array is considered for endfire scanning of main beam only along the four diagonal directions (i.e., the main beam is scanned in 90° steps).

2.2.1 Array Factor

A four-element planar array in a 2 × 2 grid arrangement can be used to achieve the 360° lateral scan in 90° steps. A 2 × 2 grid arrangement of four isotropic elements a_1, a_2, a_3, and a_4 forming a planar array is shown in Figure 2.1. In the far-field, the array factor AF of the planar array with uniform unit amplitude excitation and ignoring coupling between the elements [21] is given by

$$\begin{aligned} \mathrm{AF}(\theta,\phi) &= \left\{e^{j(k_0 d_x \sin\theta\cos\phi+\beta_x)/2} + e^{-j(k_0 d_x \sin\theta\cos\phi+\beta_x)/2}\right\} \\ &\quad \times \left\{e^{j(k_0 d_y \sin\theta\sin\phi+\beta_y)/2} + e^{-j(k_0 d_y \sin\theta\sin\phi+\beta_y)/2}\right\} \\ &= 4\cos\left(\frac{k_0 d_x \sin\theta\cos\phi+\beta_x}{2}\right)\cos\left(\frac{k_0 d_y \sin\theta\sin\phi+\beta_y}{2}\right) \end{aligned} \tag{2.1}$$

where $k_0 = 2\pi/\lambda_0$ is the free-space wavenumber at the wavelength λ_0 (= 5 mm at 60 GHz), d_x and d_y are the interelement separations in the x- and y-directions in the azimuth plane, θ and ϕ are the elevation and azimuth observation angles, and β_x and β_y are the interelement phase shifts in the x- and y-directions, respectively.

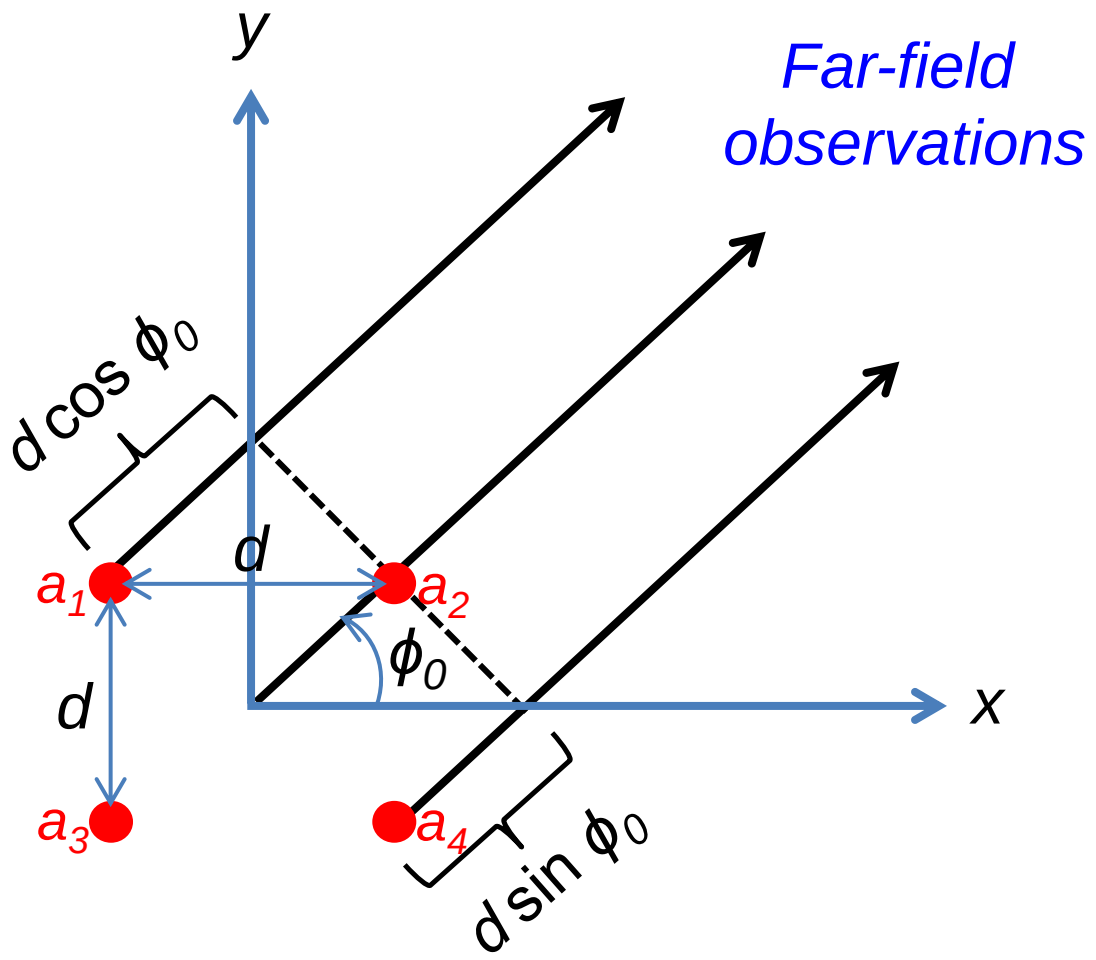


Figure 2.1. Planar array of four isotropic antenna elements in a 2 × 2 grid arrangement in the azimuth plane [13].

In the presence of an infinite ground plane, the AF can be derived by applying image theory to (2.1) [21]. Each isotropic element is assumed to be a vertical electric source at a height $z = h/2$ above an infinite perfect electric conductor (PEC). The AF with the ground plane considered, is then given by

$$\begin{aligned} \mathrm{AF}(\theta,\phi) = 8\cos\left(\frac{k_0 d_x \sin\theta\cos\phi+\beta_x}{2}\right)\cos\left(\frac{k_0 d_y \sin\theta\sin\phi+\beta_y}{2}\right) \\ \times\cos\left(\frac{kh}{2}\cos\theta\right) \end{aligned} \tag{2.2}$$

where the AF is valid only above the ground plane ($z \geq 0$) i.e, $-90 \leq \theta \leq 90°$.

The normalized array factor AF_n, from (2.2), can be written as

$$\mathrm{AF}_n(\theta,\phi) = \cos\left(\frac{k_0 d_x \sin\theta\cos\phi + \beta_x}{2}\right)\cos\left(\frac{k_0 d_y \sin\theta\sin\phi + \beta_y}{2}\right) \times \cos\left(\frac{kh}{2}\cos\theta\right) \tag{2.3}$$

From (2.3), the interelement phase shifts required to have the main beam of the array sweep along the four diagonal directions i.e., $\phi_0 = 45°$, $-45°$, $135°$, and $-135°$ in the azimuth plane ($\theta_0 = 90°$, i.e., endfire condition for a planar array) are given by

$$\beta_x = \beta_{a_{2,1}} = \beta_{a_{4,3}} = -k_0 d_x \cos\phi_0 \tag{2.4}$$

$$\beta_y = \beta_{a_{2,4}} = \beta_{a_{1,3}} = -k_0 d_y \sin\phi_0 \tag{2.5}$$

Substituting the four different values for ϕ_0 in (2.4) and (2.5) with $d_x = d_y = d$ yields four different combinations of β_x and β_y which are listed in Table 2.1.

Table 2.1. Interelement phase shifts required for main beam formation in the azimuth plane [13]

$\boldsymbol{\phi_0}$	$\boldsymbol{\beta_x}$		$\boldsymbol{\beta_y}$	
$+45°$	$-k_0 d/\sqrt{2}$	$-90°$	$-k_0 d/\sqrt{2}$	$-90°$
$+135°$	$+k_0 d/\sqrt{2}$	$+90°$	$-k_0 d/\sqrt{2}$	$-90°$
$-135°$	$+k_0 d/\sqrt{2}$	$+90°$	$+k_0 d/\sqrt{2}$	$+90°$
$-45°$	$-k_0 d/\sqrt{2}$	$-90°$	$+k_0 d/\sqrt{2}$	$+90°$

2.2.2 Main Beam Formation

For the phase shifts given in (2.4) and (2.5), only the array factor is maximized in the azimuth plane (i.e., endfire) along ϕ_0. The element pattern has to be considered as well. The total far-zone electric field of the array $\vec{E}_{\text{total}}$ is the product of the field of a single element $\vec{E}_{\text{single}}$ and the array factor AF [21], expressed as

$$\vec{E}_{\text{total}}(\theta,\phi) = \vec{E}_{\text{single}}(\theta,\phi)\mathrm{AF}(\theta,\phi) \tag{2.6}$$

The element far-field can be decomposed into vertical E_θ and horizontal E_ϕ polarization components as follows:

$$\vec{E}_{\text{single}}(\theta, \phi) = E_\theta \hat{a}_\theta + E_\phi \hat{a}_\phi \tag{2.7}$$

The array factor by itself is derived using isotropic elements and does not consider the directional and polarization characteristics of the antenna elements. The pattern multiplication in (2.6) incorporates the directional and polarization characteristics of the antenna elements into the total field.

The interelement separations, d_x and d_y, in the azimuth plane are set so that the main beams in the four diagonal directions are obtained with $\pm 90^\circ$ interelement phase shifts. That is,

$$|\beta_x| = |\beta_y| = \pi/2 = 90^\circ \tag{2.8}$$

which can be achieved by setting

$$d_x = d_y = d = 0.3535\lambda_0 \tag{2.9}$$

Since $d < \lambda_0$, the grating lobes are avoided as well [21]. The 90° value is chosen as it can be easily obtained at the output of the quadrature (90°) hybrid couplers. This would be helpful in designing feed network based on these couplers [59], as will be discussed in more detail in Chapter 3. With (2.8) and (2.9) satisfied, β_x and β_y must cycle through four different combinations of $\pm 90^\circ$ values listed in Table 2.1, obtained for four different values of main beam angles ϕ_0 along the diagonal directions.

The maximum directivity D_0 of the planar array will be in the azimuth plane ($\theta_0 = 90^\circ$) along ϕ_0 direction, and can be calculated as [21]

$$D_0(\theta_0, \phi_0) = \frac{4\pi}{\int_{\phi=0}^{2\pi} \int_{\theta=0}^{\pi/2} |\text{AF}_n(\theta, \phi)|^2 \sin\theta d\theta d\phi} \tag{2.10}$$

where $\text{AF}_n(\theta, \phi)$ is substituted from (2.3) and the denominator can be numerically evaluated using the trapezoidal integration method in Matrix Laboratory (MATLAB).

The normalized radiation intensity U_n of the array is given by [21]

$$U_n(\theta, \phi) = |\mathrm{AF}_n(\theta, \phi)|^2 \tag{2.11}$$

The directivity D of the array in any direction (θ, ϕ) can be written as [21]

$$D(\theta, \phi) = D_0 U_n(\theta, \phi) \tag{2.12}$$

The 3-D plot of the directivity $D(\theta, \phi)$ of the planar array of isotropic elements with $d = 0.37\lambda_0$ and $\phi_0 = 135^\circ$, is shown in Figure 2.2(a). The d chosen is slightly larger than that given in (2.9) to meet the minimum trace spacing fabrication requirement when actual elements are chosen later in Section 2.3. The main beam direction is along $(\theta_0, \phi_0) = (90^\circ, 135^\circ)$, as can be seen from the vertical and horizontal plane patterns in Figure 2.2(b) and (c), respectively.

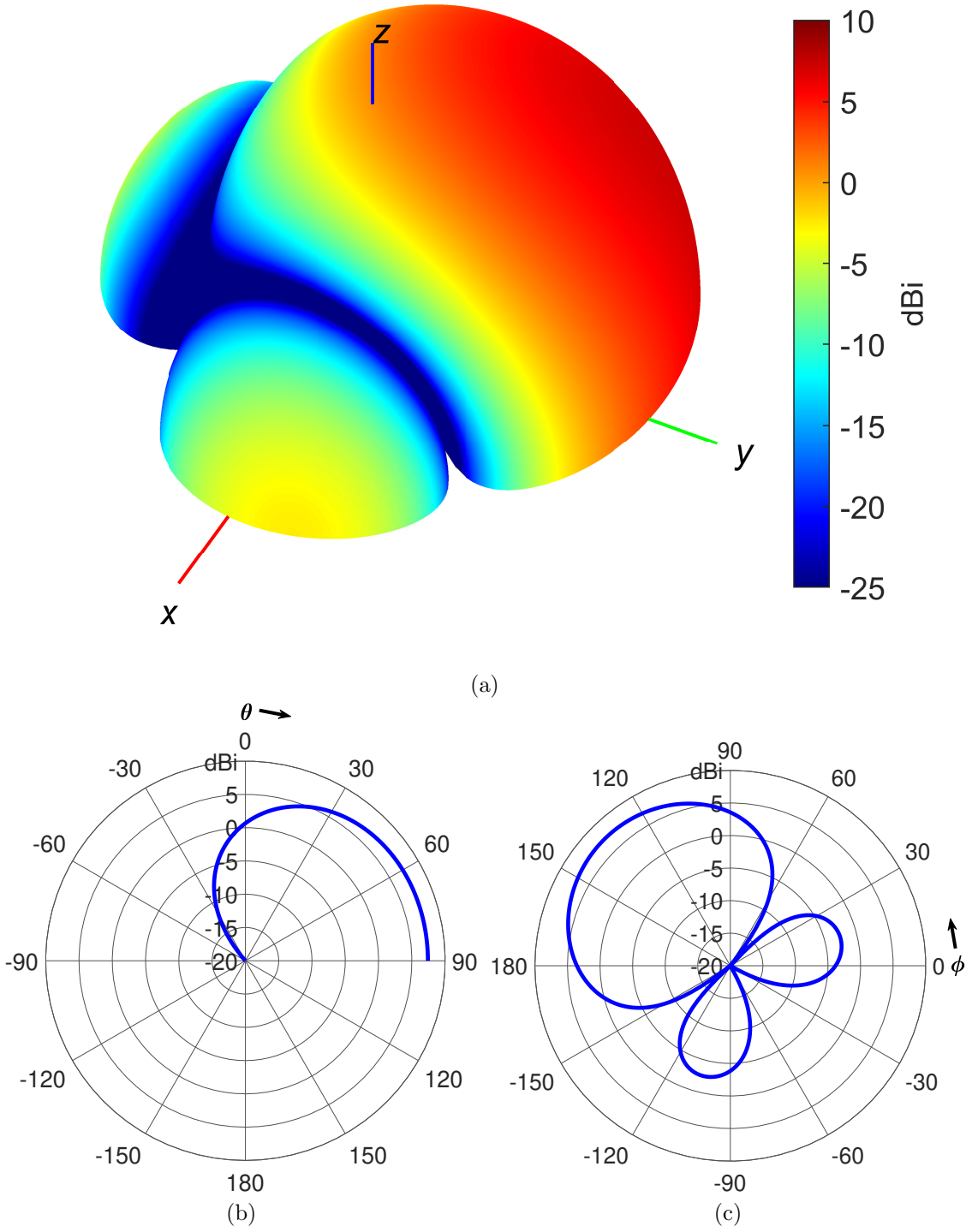


Figure 2.2. Directivity patterns (dBi) of the 2 × 2 planar array of isotropic elements above an infinite ground plane. (a) 3-D pattern. (b) Vertical plane pattern ($\phi = 135°$). (c) Horizontal plane pattern ($\theta = 90°$).

The maximum directivity D_0, half-power beamwidth (HPBW), first-null beamwidth (FNBW), and maximum side lobe level (SLL) of the planar array, in the horizontal plane, are listed in Table 2.2.

Table 2.2. Maximum directivity, HPBW, FNBW, and SLL of the 2 × 2 planar array of isotropic elements above an infinite ground plane

Metric	**Value**
Maximum directivity (D_0)	7.41 dBi
Horizontal plane HPBW	82°
Horizontal plane FNBW	170°
Horizontal plane max. SLL	10 dB

Ideally, for the interchip communication illustrated in Figure 1.8, it is desirable to have the maximum of both the element field and array factor lie in the azimuth plane ($\theta = 90°$). This is the endfire maximum condition. From (2.6), it is easy to see that this would maximize the total far-zone field in the azimuth plane along ϕ_0 directions provided (2.4) and (2.5) are satisfied and therefore maximize interchip transmission. Hence, maximizing just the array factor is sub-optimal. The element field must also be maximized by choosing antenna elements that have good lateral radiation. However, printed antenna elements that have endfire radiation are hard to realize in the presence of an unavoidable ground plane [23]. Vias can be incorporated into the antenna element to realize a monopole-like pattern and improve the lateral radiation. However, larger ground planes are required to move the element pattern maximum toward the azimuth plane [21]. Due to the limited chip size, the ground planes cannot be made arbitrarily large. Thus, there is a tradeoff between the antenna performance and geometry.

In summary, the selection of antenna element is dictated by the need to maximize lateral radiation (in the azimuth plane). MS antennas such as the rectangular and circular patch that have their pattern maximum in the vertical plane are not optimized for lateral transmission. Furthermore, to get good impedance matching, these

antennas must be probe fed off center. This results in azimuthal asymmetry in the element radiation pattern. The asymmetric probe radiation can result in unwanted side lobes [21].

2.3 Center-Fed Circular Patch With Side Vias

In light of these issues, a center-fed circular patch with symmetrically placed side vias around the center is proposed as the antenna element. Such circular patches have been used at low frequencies to reduce mutual coupling due to surface waves [60] and improve pattern smoothness [61]. In this dissertation, the circular patches are designed so that they enhance rather than reduce the surface wave excitation [60]. There are four side vias around the center feed, which serve to improve impedance matching. The location of side vias must be optimized to improve matching since the center feed via cannot be moved to change the input impedance. The vias maintain azimuthal symmetry in the element pattern if their distances from the patch center are kept the same. In addition, the side vias improve lateral radiation because they cause the pattern maximum to move away from vertical and toward the horizontal plane.

2.3.1 Antenna Structure

The 3-D model of the center-fed circular patch with four side vias, created in High Frequency Structural Simulator (HFSS), is shown in Figure 2.3. Rogers RO4003C is used as the antenna substrate [62], a low-loss hydrocarbon ceramic with dielectric constant (ϵ_r) of 3.55 and loss tangent ($\tan\delta$) of 0.0027. The diameter of the circular patch a is 1.8 mm. The radial locations of the vias b defined from the patch center to the via centers are 0.61 mm each. The diameters of the center feed via and four side vias a_f are 0.15 mm each. These are optimized values for the patch element to make it resonate with good match at 60 GHz. The length and the width of the ground

plane are each set to $W_g = 7.3$ mm. The side view of the antenna structure with the stackup of the layers is shown in Figure 2.3(c). There are two conductor layers: antenna and ground plane. The layers are separated from one another by a RO4003C laminate. The laminate thickness h is 0.2 mm. The thickness t of printed copper is 35 μm for both the antenna and ground planes.

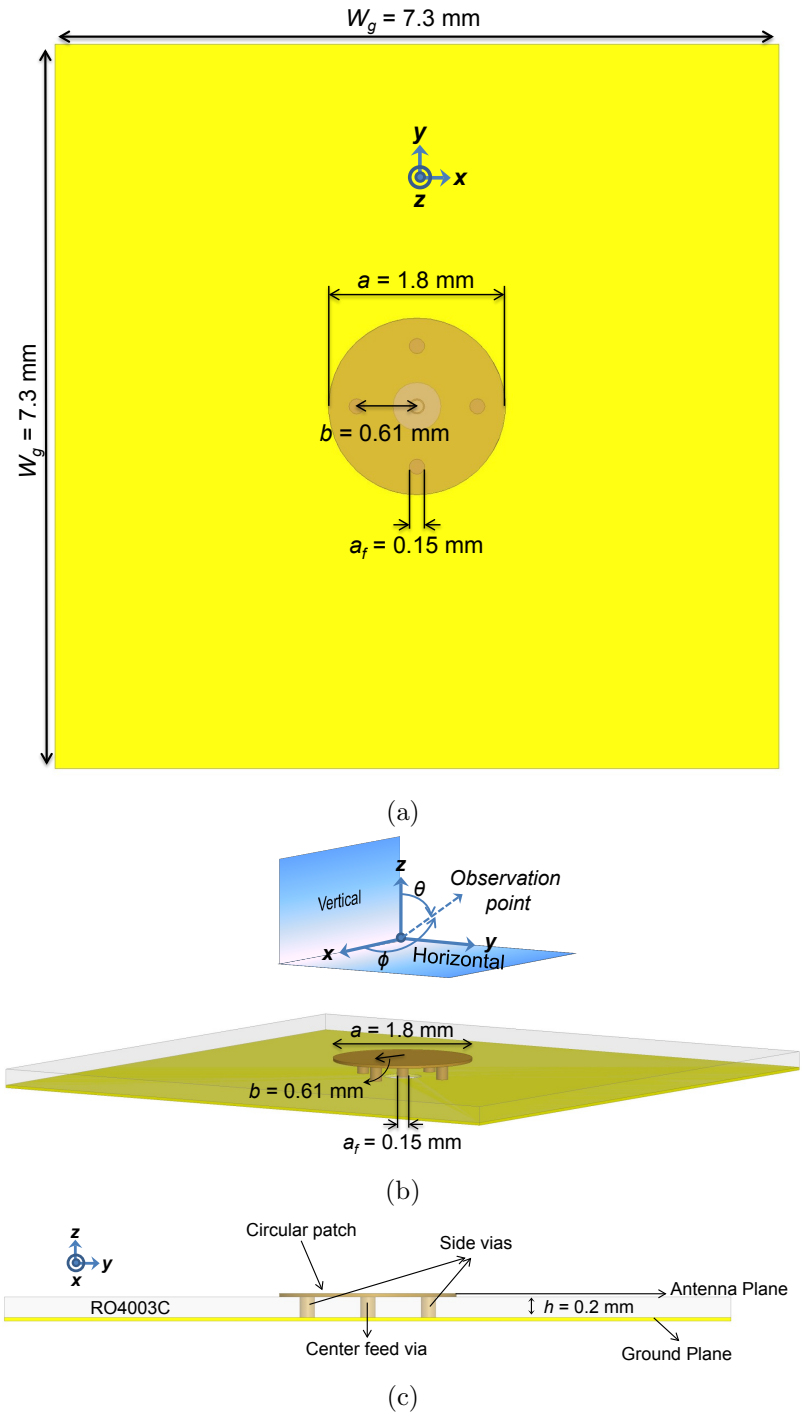


Figure 2.3. 3-D model of the center-fed circular patch with four side vias [13]. (a) Top view. (b) Perspective view showing the vertical and horizontal planes. (c) Stackup view.

2.3.2 Cavity Model

The center-fed circular patch with side (shorting) vias can be represented as a cavity with two concentric regions: inner region 1 and outer region 2, as depicted in Figure 2.4. The region 1 is defined by $a_f/2 \leq \rho \leq b$ where $a_f/2$ is the radius of the center feed via and b is the radial distance of the shorting vias' center from the patch center. Region 1 thus exists between the center feed via and the shorting vias. The surface of the center feed via can be represented as a cylindrical sheet of source current that flows along the z-direction with uniform surface current density J_{sz} given by [63]

$$\vec{J}_s = J_{sz}\hat{z} = \frac{I_0}{\pi a_f}\delta\left(\rho - \frac{a_f}{2}\right)\hat{z} \tag{2.13}$$

where I_0 is the feed current.

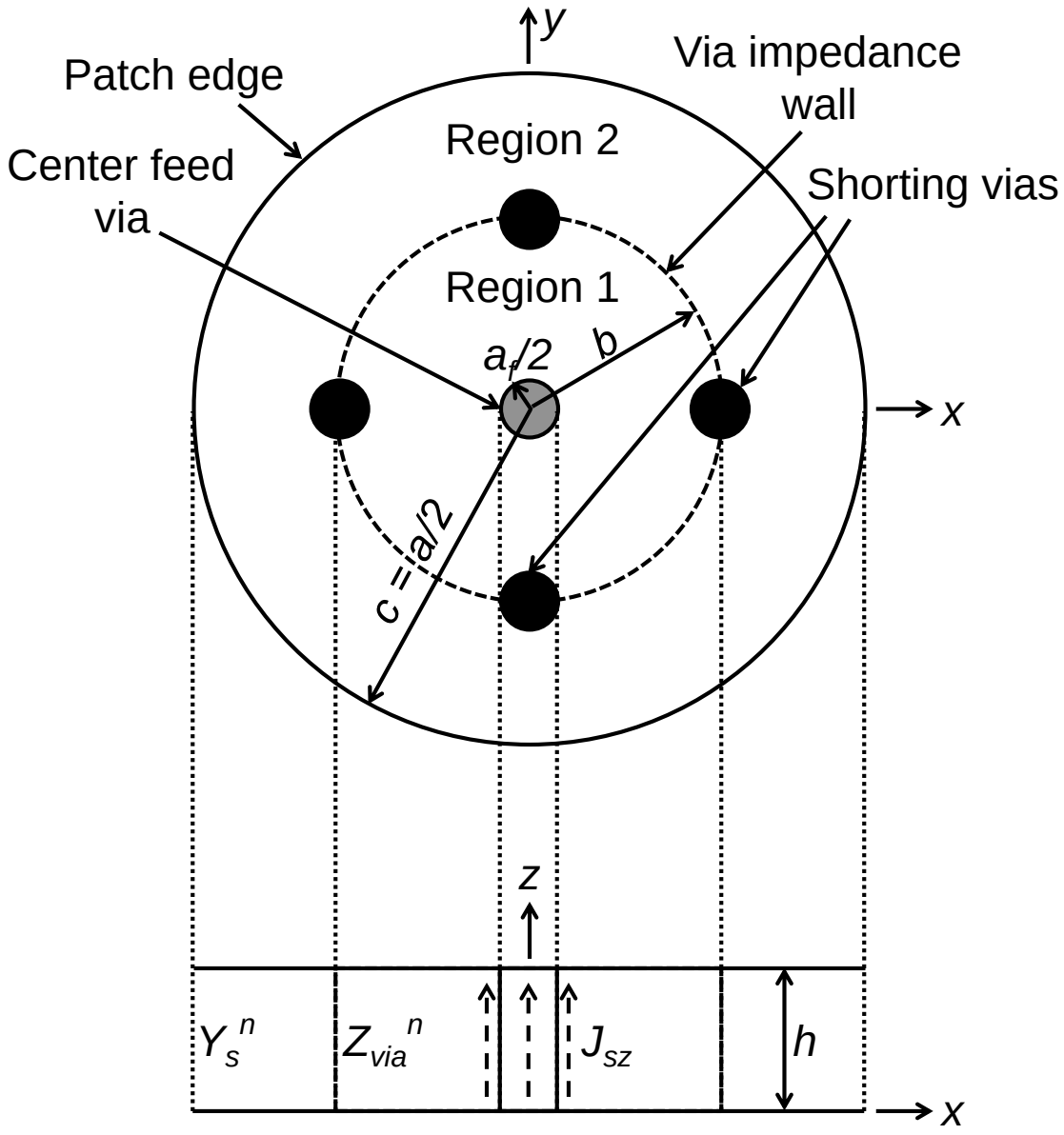


Figure 2.4. Cavity model of the center-fed circular patch [63, 64].

To simplify the modeling process, the wall formed by the shorting vias can be modeled as a continuous cylindrical sheet [63], having a sheet impedance Z^n_{via} [65] given by

$$Z^n_{via} = j\omega L_s \tag{2.14}$$

where n represents the azimuthal (ϕ) modenumber of the dominant mode, ω is the angular frequency, and L_s^n is the sheet inductance of the via wall. A method to calculate L_s^n is given in [65]. Similarly, the patch edge can be represented as another cylindrical sheet at a radial distance $c = a/2$ from the center, having a surface admittance Y_s^n, containing both real and imaginary parts as follows [66]:

$$\begin{aligned} Y_s^n &= G_s^n + jB_s^n \\ &= G_{sp}^n + G_{sw}^n + jB_s^n \qquad n = 0, 1, 2, ... \end{aligned} \tag{2.15}$$

where the real part G_s^n is the sum of the surface conductances G_{sp}^n and G_{sw}^n due to the energy lost in radiation and surface waves, respectively, and the imaginary part is the surface susceptance B_s^n due to the energy stored in the fringing fields at the patch edge. The region 2 is defined by $b \leq \rho \leq c$, and thus exists between the shorting vias and the patch edge. The source and boundary conditions can be enforced if Z_{via}^n and Y_s^n are known. Y_s^n is calculated using the spectral domain analysis, as presented in Section 2.3.3.

The mode-matching techniques can then be applied to the cavity model to determine the coefficients of the electric fields in both the regions. This enables the derivation of an analytical expression for the input impedance Z_{in} of the antenna. At 60 GHz, $h \ll \lambda_0$ and the field variation in the z-direction can be ignored (i.e., $p = 0$ for the z modenumber). The field components of these modes in the two regions are as follows:

Region 1: $a_f/2 \leq \rho \leq b$

$$E_{z1} = \sum_{n=0}^{\infty} \left[A_n J_n(k_1'\rho) + B_n Y_n(k_1'\rho)\right] \cos(n\phi) \tag{2.16}$$

$$H_{\rho 1} = \frac{1}{j\omega\mu_0\rho} \sum_{n=0}^{\infty} n \left[A_n J_n(k_1'\rho) + B_n Y_n(k_1'\rho)\right] \sin(n\phi) \tag{2.17}$$

$$H_{\phi 1} = \frac{k_1'}{j\omega\mu_0} \sum_{n=0}^{\infty} \left[A_n J_n'(k_1'\rho) + B_n Y_n'(k_1'\rho)\right] \cos(n\phi) \tag{2.18}$$

Region 2: $b \leq \rho \leq c$

$$E_{z2} = \sum_{n=0}^{\infty} [C_n J_n(k_1'\rho) + D_n Y_n(k_1'\rho)] \cos(n\phi) \tag{2.19}$$

$$H_{\rho 2} = \frac{1}{j\omega\mu_0\rho} \sum_{n=0}^{\infty} n\,[C_n J_n(k_1'\rho) + D_n Y_n(k_1'\rho)] \sin(n\phi) \tag{2.20}$$

$$H_{\phi 2} = \frac{k_1'}{j\omega\mu_0} \sum_{n=0}^{\infty} [C_n J_n'(k_1'\rho) + D_n Y_n'(k_1'\rho)] \cos(n\phi) \tag{2.21}$$

where $J_n(k_1'\rho)$ and $Y_n(k_1'\rho)$ are the Bessel functions of the first and second kind, respectively, of order n, the prime ($'$) indicates the derivative with respect to the whole argument, and

$$k_1' = k_0\sqrt{\epsilon_r'} \tag{2.22}$$

where ϵ_r' is the complex dielectric constant of the antenna substrate given by

$$\epsilon_r' = \epsilon_r(1 - j\tan\delta_{eff}) \tag{2.23}$$

and $\tan\delta_{eff}$ is the effective loss tangent, which takes into account both dielectric loss tangent ($\tan\delta$) and conductor skin depth losses due to finite conductivity σ, written as [67]

$$\tan\delta_{eff} = \tan\delta + \frac{1}{h}\sqrt{\frac{1}{\pi\mu_0\sigma f}} \tag{2.24}$$

The field coefficients A_n, B_n, C_n, and D_n can be found by enforcing a set of independent boundary conditions as follows [63]:

Enforced Boundary Conditions

1. H_ϕ is discontinuous at $\rho = a_f/2$ due to the excitation surface current $\vec{J}_s$ on the center via. The magnetic field $\vec{H}_0$ inside the via is zero and so

$$\hat{a}_\rho \times [\vec{H}_1 - \vec{H}_0] = \vec{J}_s\Big|_{\rho=a_f/2}$$

$$H_{\phi 1}(a_f/2) = J_{sz}$$

$$-\frac{j}{\eta}\sum_{n=0}^{\infty} [A_n J_n'(k_1'a_f/2) + B_n Y_n'(k_1'a_f/2)] \cos(n\phi) = \frac{I_0}{\pi a_f}\delta\left(\rho - \frac{a_f}{2}\right)$$

$$-\frac{j}{\eta}\left[A_n J_n'(k_1' a_f/2) + B_n Y_n'(k_1' a_f/2)\right] = \frac{2I_0}{(1+\delta_n)\pi a_f}\,\mathrm{sinc}(2\pi n) \tag{2.25}$$

where

$$\delta_n = \begin{cases} 1 & \text{for } n = 0 \\ 0 & \text{for } n > 0 \end{cases}$$

2. E_z^n is continuous at $\rho = b$.

$$\hat{a}_\rho \times \vec{E}_1^n = \hat{a}_\rho \times \vec{E}_2^n\Big|_{\rho=b}$$
$$E_{z1}^n(b) = E_{z2}^n(b)$$

$$\left[A_n J_n(k_1' b) + B_n Y_n(k_1' b)\right] - \left[C_n J_n(k_1' b) + B_n Y_n(k_1' b)\right] = 0 \tag{2.26}$$

3. H_ϕ^n is discontinuous at $\rho = b$ due to the induced surface current $\vec{J}_{via}^n$ on the shorting vias.

$$\hat{a}_\rho \times [\vec{H}_2^n - \vec{H}_1^n] = \vec{J}_{via}^n\Big|_{\rho=b}$$
$$\vec{J}_{via}^n = \frac{\vec{E}_{z1}^n}{Z_{via}^n}\Big|_{\rho=b}$$
$$H_{\phi 2}^n(b) - H_{\phi 1}^n(b) = \frac{E_{z1}^n(b)}{Z_{via}^n}$$

$$A_n\left[\frac{j}{\eta}J_n'(k_1' b) - \frac{J_n(k_1' b)}{Z_{via}^n}\right] + B_n\left[\frac{j}{\eta}Y_n'(k_1' b) - \frac{Y_n(k_1' b)}{Z_{via}^n}\right]$$
$$-\frac{j}{\eta}\left[C_n J_n'(k_1' b) + D_n Y_n'(k_1' b)\right] = 0 \tag{2.27}$$

4. The admittance boundary condition at $\rho = c$ is

$$H_{\phi 2}^n(c) = -Y_s^n E_{z2}^n(c)$$

$$C_n\left[-\frac{j}{\eta}J_n'(k_1' c) + Y_s^n J_n(k_1' c)\right] + D_n\left[-\frac{j}{\eta}Y_n'(k_1' c) + Y_s^n Y_n(k_1' c)\right] = 0 \tag{2.28}$$

The equations (2.25) through (2.28) can be written in the matrix form as [63]

$$\big[F\big]\,\big[g\big] = \big[h\big] \tag{2.29}$$

where $[F]$ is a 4×4 matrix, $[g]$ and $[h]$ are both 4×1 column vectors. Each is given by

$$[F] = \begin{bmatrix} -\frac{j}{\eta}J_n'(k_1'a_f/2) & -\frac{j}{\eta}Y_n'(k_1'a_f/2) & 0 & 0 \\ J_n(k_1'b) & Y_n(k_1'b) & -J_n(k_1'b) & -Y_n(k_1'b) \\ \frac{j}{\eta}J_n'(k_1'b) - \frac{J_n(k_1'b)}{Z_{via}^n} & \frac{j}{\eta}Y_n'(k_1'b) - \frac{Y_n(k_1'b)}{Z_{via}^n} & -\frac{j}{\eta}J_n'(k_1'b) & -\frac{j}{\eta}Y_n'(k_1'b) \\ 0 & 0 & -\frac{j}{\eta}J_n'(k_1'c) + Y_s^n J_n(k_1'c) & -\frac{j}{\eta}Y_n'(k_1'c) + Y_s^n Y_n(k_1'c) \end{bmatrix} \tag{2.30}$$

$$[g] = \begin{bmatrix} A_n \\ B_n \\ C_n \\ D_n \end{bmatrix} \tag{2.31}$$

$$[h] = \begin{bmatrix} \frac{2I_0}{(1+\delta_n)\pi a_f}\,\mathrm{sinc}(2\pi n) \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.32}$$

Equation (2.29) can be solved for $[g]$ to determine the field coefficients. When the electric field on the surface of the feed via $E_{z1}(a_f/2, \phi)$ is determined, the input impedance Z_{in} of the antenna can be calculated as follows [63]:

$$Z_{in} = -\frac{1}{|I_0|^2}\int_S E_{z1}(a_f/2, \phi) J_{sz}^* dS \tag{2.33}$$

where the integration is to be carried out around the cylindrical surface S of the center feed via and $I_0 = 1$ A can be set without the loss of generality. Evaluating (2.16) at $\rho = a_f/2$, and using it and J_{sz} from (2.13) in (2.33),

$$\begin{aligned} Z_{in} &= -\frac{1}{2}\int_{\phi=0}^{2\pi}\int_{z=0}^{h} E_{z1}(a_f/2, \phi) J_{sz}^* a_f \, d\phi \, dz \\ &= -\frac{h}{2}\int_{\phi=0}^{2\pi} E_{z1}(a_f/2, \phi) J_{sz}^* a_f d\phi \\ &= -\frac{h}{2\pi}\sum_{n=0}^{\infty}\left[A_n J_n(k_1'a_f/2) + B_n Y_n(k_1'a_f/2)\right]\left[\frac{\sin(n\phi)}{n}\right]_0^{2\pi} \\ &= -h\sum_{n=0}^{\infty}\left[A_n J_n(k_1'a_f/2) + B_n Y_n(k_1'a_f/2)\right]\mathrm{sinc}(2\pi n) \\ Z_{in} &= -h\left[A_0 J_0(k_1'a_f/2) + B_0 Y_0(k_1'a_f/2)\right] \end{aligned} \tag{2.34}$$

Equation (2.34) indicates that only the $n = 0$ azimuthal mode contributes to the input impedance and is the dominant mode. This is to be expected since the excitation current density assumed in (2.13) has no azimuthal (ϕ) variation and can only excite the $n = 0$ mode. For this mode, the sheet inductance is calculated to be $L_s^0 = 107$ pH using the electric field integral equation (EFIE) developed in [65]. Equation (2.34) does not include the capacitive $-jX_c$ due to the DC mode capacitance C_0 [68] of the center-fed circular patch, which is given by

$$X_c = \frac{1}{\omega C_0} \tag{2.35}$$

where

$$C_0 = \frac{\epsilon_0 \epsilon_r \pi \left[c^2 - 5(0.5a_f)^2\right]}{h} \tag{2.36}$$

After adding $-jX_c$, (2.34) takes the following final form:

$$Z_{in} = -h\left[A_0 J_0(k_1' a_f/2) + B_0 Y_0(k_1' a_f/2)\right] - jX_c \tag{2.37}$$

2.3.3 Determination of Surface Admittance

The surface admittance Y_s^n for circular geometries can be determined by using spectral domain analysis [60, 66]. In the cavity model shown in Figure 2.4, an equivalent magnetic surface current is assumed at the patch edge and the effect of the dielectric substrate is taken into account. Therefore, the energy lost due to both radiation and surface waves are incorporated. The surface admittance Y_s^n can be written as [60,66]

$$Y_s^n = ch \int_{k_\rho=0}^{\infty} I_v^{TM}(k_\rho)\left[J_n'(k_\rho c)\right]^2 k_\rho dk_\rho + \frac{hn^2}{c}\int_{k_\rho=0}^{\infty} \frac{I_v^{TE}(k_\rho) J_n^2(k_\rho c)}{k_\rho} dk_\rho \tag{2.38}$$

where

$$I_v^{TM}(k_\rho) = \frac{Z_1^{TM} + jZ_0^{TM}\tan\left(\frac{k_z h}{2}\right)}{Z_0^{TM} Z_1^{TM}\left[1 - \tan^2\left(\frac{k_z h}{2}\right)\right] + j2(Z_1^{TM})^2 \tan\left(\frac{k_z h}{2}\right)} \tag{2.39}$$

$$I_v^{TE}(k_\rho) = \frac{Z_1^{TE} + jZ_0^{TE}\tan\left(\frac{k_z h}{2}\right)}{Z_0^{TE} Z_1^{TE}\left[1 - \tan^2\left(\frac{k_z h}{2}\right)\right] + j2(Z_1^{TE})^2 \tan\left(\frac{k_z h}{2}\right)} \tag{2.40}$$

$$k_{z0} = \sqrt{k_0^2 - k_\rho^2} \tag{2.41}$$

$$k_z = \sqrt{k_1^2 - k_\rho^2} \tag{2.42}$$

$$k_1 = k_0\sqrt{\epsilon_r} \tag{2.43}$$

$$Z_0^{TM} = \frac{k_{z0}}{\omega\epsilon_0} \tag{2.44}$$

$$Z_1^{TM} = \frac{k_z}{\omega\epsilon_r\epsilon_0} \tag{2.45}$$

$$Z_0^{TE} = \frac{\omega\mu_0}{k_{z0}} \tag{2.46}$$

$$Z_1^{TE} = \frac{\omega\mu_0}{k_z} \tag{2.47}$$

The TM and TE represent the quantities associated with the transverse magnetic (TM) and transverse electric (TE) modes, respectively. The integrals in (2.38) can be numerically evaluated in the range $0 \leq k_\rho \leq k_0$ and the real part gives the surface conductance due to radiation G_{sp}^n as follows [66]:

$$G_{sp}^n = ch\mathrm{Re}\left[\int_{k_\rho=0}^{k_0} I_v^{TM}(k_\rho)\left[J_n'(k_\rho c)\right]^2 k_\rho dk_\rho\right] + \frac{hn^2}{c}\mathrm{Re}\left[\int_{k_\rho=0}^{k_0} \frac{I_v^{TE}(k_\rho)J_n^2(k_\rho c)}{k_\rho} dk_\rho\right] \tag{2.48}$$

In the range $k_0 \leq k_\rho \leq k_1$, depending on the angular frequency ω and substrate parameters, the first integral in (2.38) has at least one or more singular points that are associated with the TM_m^z surface wave modes [66], where m is the radial (ρ) modenumber. The second integral in (2.38) may also have singular points and they are associated with the TE_m^z surface wave modes. Nonetheless, for the dominant $n = 0$ mode, the second integral vanishes and does not contribute at all to the surface admittance, as (2.38) indicates. For the frequency range and substrate parameters considered in this dissertation, only the TM_0^z surface wave mode is propagating with the wavenumber $k_\rho = k_{TM_0}$. Therefore, the first integral in (2.38) has a singular

point at $k_\rho = k_{TM_0}$. After extracting the residue of the integral at the singular point, the surface conductance due to the TM_0^z surface wave G_{sw}^n can be calculated as follows [60]:

$$G_{sw}^n = -j\pi ch k_0 k_{TM_0} \mathrm{Res}\{I_v^{TM}(k_{TM_0})\} \left[J_n'(k_{TM_0}c)\right]^2 \tag{2.49}$$

where the residue is given by

$$\mathrm{Res}\{I_v^{TM}(k_{TM_0})\} = \frac{Z_1^{TM} + jZ_0^{TM}\tan\left(\frac{k_z h}{2}\right)}{D'(k_{TM_0})} \tag{2.50}$$

where $D'(k_{TM_0})$ represents the derivative of the denominator in (2.39) with respect to k_ρ evaluated at k_{TM_0}. It can be written as

$$D'(k_{TM_0}) = D_1' + D_2' + D_3' \tag{2.51}$$

where

$$D_1' = -\frac{k_{TM_0}\eta_0^2}{k_0\epsilon_r}\left[\frac{k_z}{k_{z0}} + \frac{k_{z0}}{k_z}\right] \tag{2.52}$$

$$D_2' = \frac{k_{TM_0}\eta_0^2}{k_0\epsilon_r}\left[\left(\frac{k_z}{k_{z0}} + \frac{k_{z0}}{k_z}\right)\tan^2\left(\frac{k_z h}{2}\right) + hk_{z0}\tan\left(\frac{k_z h}{2}\right)\sec^2\left(\frac{k_z h}{2}\right)\right] \tag{2.53}$$

$$D_3' = -\frac{j4k_{TM_0}\eta_0^2}{k_0\epsilon_r}\left[\tan\left(\frac{k_z h}{2}\right) + \frac{k_z h}{4}\sec^2\left(\frac{k_z h}{2}\right)\right] \tag{2.54}$$

The singular point at k_{TM_0} is obtained numerically as the root of the following equation [60, 66]:

$$\frac{j\omega}{I_v^{TM}(k_{TM_0})} = 0 \tag{2.55}$$

The k_{TM_0} is solved for at each frequency point and the calculated values are plotted in Figure 2.5.

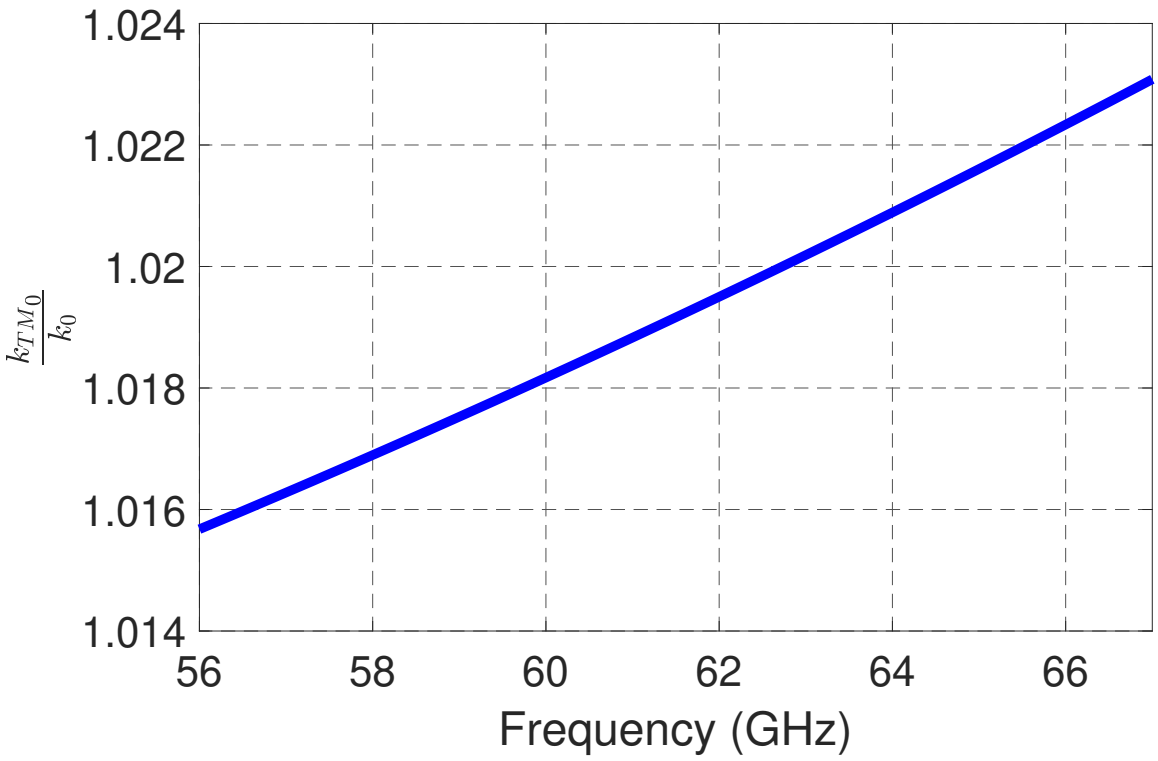


Figure 2.5. The normalized wavenumber k_{TM_0}/k_0 of the TM_0^z surface wave mode increases with frequency.

Note that although the dielectric and conductor losses are taken into account for Z_{in} calculation, they are ignored for Y_s^n calculation. The integrals in (2.38) are purely imaginary in the range $k_1^+ \leq k_\rho < \infty$ and contribute to the surface susceptance B_s^n [66] as follows:

$$B_s^n = -jch\left[k_0 L_v^{TM}(k_{TM_0}) \ln\left(\frac{k_1 - k_{TM_0}}{k_{TM_0} - k_0}\right) + k_0 \int_{k_0}^{k_1} \frac{L_v^{TM}(k_\rho) - L_v^{TM}(k_{TM_0})}{k_\rho - k_{TM_0}} dk_\rho \right.$$
$$+\mathrm{Im}\left[\int_0^{k_0} I_v^{TM}(k_\rho)\left[J_n'(k_\rho c)\right]^2 k_\rho dk_\rho + \frac{n^2}{c^2}\int_0^{k_1} \frac{I_v^{TE}(k_\rho) J_n^2(k_\rho c)}{k_\rho} dk_\rho\right]$$
$$\left. + \int_{k_1^+}^{\infty} I_v^{TM}(k_\rho)\left[J_n'(k_\rho c)\right]^2 k_\rho dk_\rho + \frac{n^2}{c^2}\int_{k_1^+}^{\infty} \frac{I_v^{TE}(k_\rho) J_n^2(k_\rho c)}{k_\rho} dk_\rho\right] \tag{2.56}$$

where

$$L_v^{TM}(k_\rho) = I_v^{TM}(k_\rho)\left[J_n'(k_\rho c)\right]^2 (k_\rho - k_{TM_0})k_\rho \tag{2.57}$$

$$L_v^{TM}(k_{TM_0}) = \mathrm{Res}\{I_v^{TM}(k_{TM_0})\}\left[J_n'(k_{TM_0} c)\right]^2 k_{TM_0} \tag{2.58}$$

The integration paths that should be used to calculate (2.48), (2.49), and (2.56), are illustrated graphically in Figure 2.6, for the dominant $n = 0$ mode.

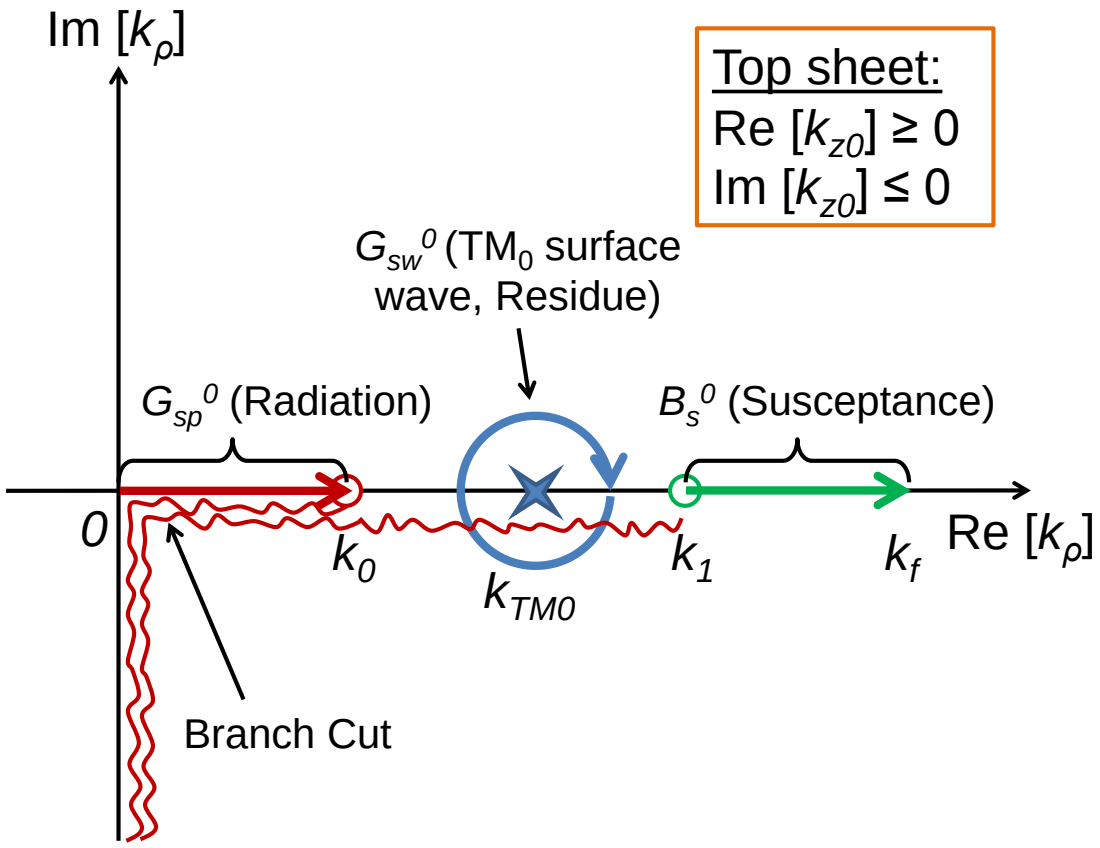


Figure 2.6. Integration paths used in evaluating the surface admittance Y_s^0 for the $n = 0$ dominant mode.

Note that the numerical integration is carried out on the top (proper) Riemann sheet so that the integrals converge [67]. To ensure that the path stays on the top sheet as k_ρ is varied, the square roots in (2.41) and (2.42) are chosen so that they

satisfy

$$\begin{aligned} \mathrm{Re}[k_{z0}] &\geq 0 \\ \mathrm{Re}[k_z] &\geq 0 \end{aligned} \tag{2.59}$$

$$\begin{aligned} \mathrm{Im}[k_{z0}] &\leq 0 \\ \mathrm{Im}[k_z] &\leq 0 \end{aligned} \tag{2.60}$$

Since the first integral in (2.48) (i.e., $I_v^{TM}(k_\rho)$) has no branch point $k_\rho = k_0$ singularities, the branch cut integration for G_{sp}^0 can be carried out on the real axis after ensuring (2.59) and (2.60). There is no need to detour above the $k_\rho = k_0$ branch point as this will only introduce numerical error in the integration. The extraction of the residue to calculate G_{sw}^0 is depicted by encircling the singular point $k_\rho = k_{TM_0}$ in Figure 2.6. Also shown in Figure 2.6 is the integration for B_s^0, which is carried out on the real axis from k_1^+ to $k_f = 311k_0\sqrt{\epsilon_r}$ in $\Delta k_\rho = 10k_0\sqrt{\epsilon_r}$ steps to achieve convergence, using the adaptive Gauss-Kronrod quadrature numerical method in MATLAB. The singularity of the integral involving $I_v^{TM}(k_\rho)$ in (2.56) at $k_\rho = k_1$ is avoided by having the start point of the integration be slightly greater than k_1, indicated mathematically by k_1^+.

The calculated surface admittance $Y_s^0 = G_{sp}^0 + G_{sw}^0 + jB_s^0$ of the dominant mode is shown in Figure 2.7. The mode has about equal contribution of space G_{sp}^0 and surface G_{sw}^0 wave components to the total conductance, as shown in Figure 2.7. Therefore, the HSSW-I is proposed in this dissertation, so that the power leaving the antenna in both forms of the waves is tapped and utilized.

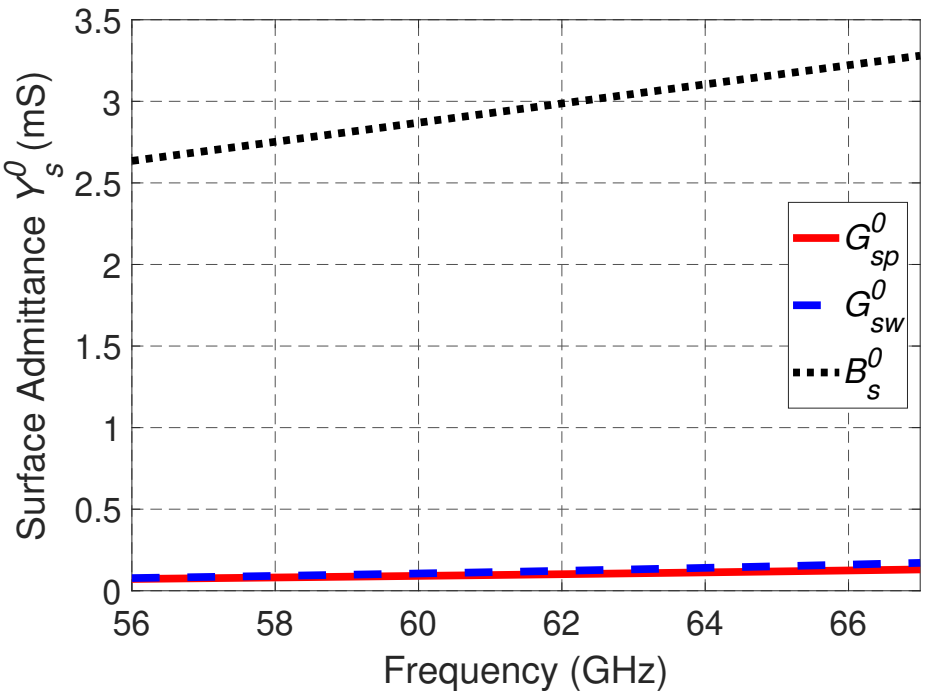
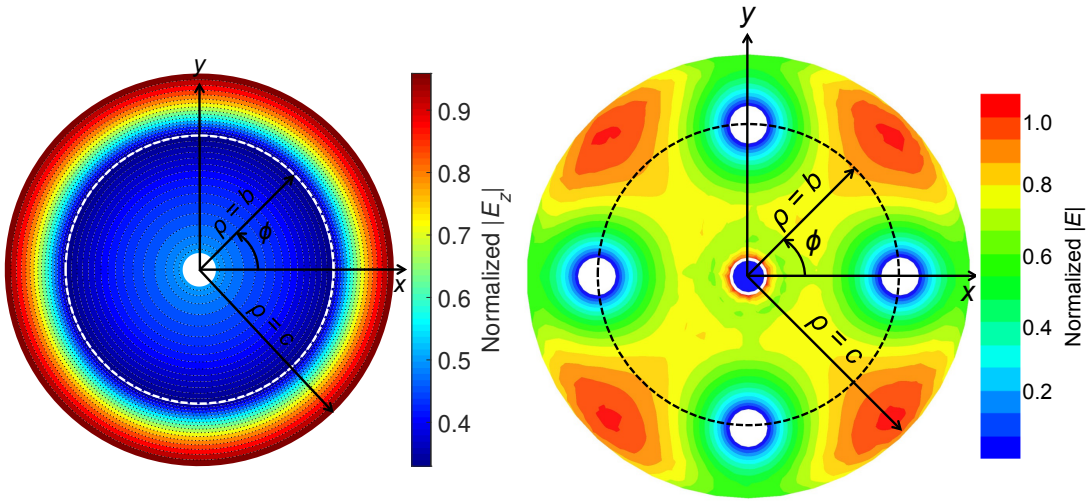


Figure 2.7. Surface admittance Y_s^0 of the dominant mode at the patch edge.

2.3.4 Dominant Mode

In the cavity model, the patch is excited at the center via with a current that has no ϕ variation, as given in (2.13). As a result, the electric and magnetic fields in the cavity also possess no ϕ variation and only the $n = 0$ term is retained in (2.16), (2.17) and so on. This is the dominant mode. The presence of the vias, however, can cause the $n = 0$ dominant term under the circular patch to vary in both ρ- and ϕ-directions. The dominant mode has no z variation because of $h \ll \lambda_0$. The field variations in the ρ, ϕ and z-directions are designated by the modenumbers m, n, and p, respectively, using the notation TM^z_{mnp}. The perturbation of the normalized electric field $|E_z|$ (under the patch) of the dominant mode along the ρ- and ϕ-directions is caused by the via wall. Figure 2.8 shows the surface plots of the electric field distribution under the patch.



(a) (b)

Figure 2.8. Surface plot of 60 GHz electric field distribution at the center horizontal plane $z = h/2$ in the substrate (under the patch). (a) Cavity model. (b) Full-wave simulation.

The ρ-direction perturbation, from the surface of the center via $\rho = a_f/2$ to the patch edge $\rho = c$, is shown in Figure 2.9. In the cavity model, $|E_z|$ is maximum at the patch edge, as shown in Figures 2.8(a) and 2.9. There is no ϕ variation of $|E_z|$ because the excitation current is of the transverse electromagnetic (TEM) type ($n = 0$). However, the ϕ variation is present in the simulated $|E_z|$, as shown in Figures 2.8(b) and 2.9. Specifically, at the patch edge $\rho = c$, the radial path $\phi = 0°$ containing the via has lower $|E_z|$ than the radial path $\phi = 45°$ with no vias. The average of the simulated $|E_z|$ of the two radial paths is also plotted in Figure 2.9 and shows a better agreement with the model $|E_z|$. The perturbations in the two ϕ-directions can be seen in the fringing fields near the patch edge. The difference in $|E_z|$ levels, however, is small, and the perturbed mode still produces a monopole-like radiation pattern, as will be shown in Section 2.3.6.

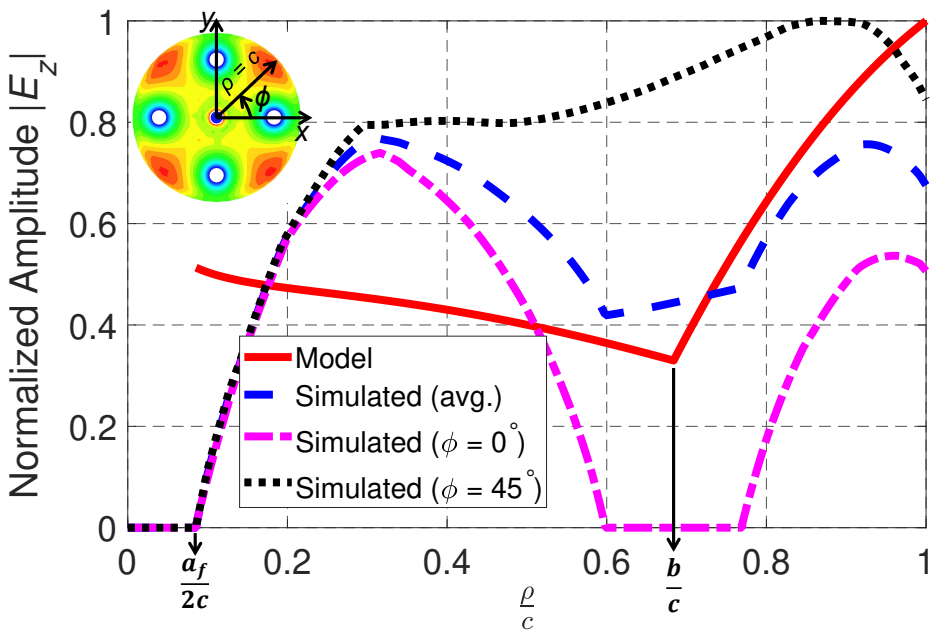


Figure 2.9. The ρ variation of normalized electric field $|E_z|$ under the center-fed circular patch.

For a circular patch with no via wall, $|E_z|$ under the patch stays constant with respect to ρ, ϕ, and z for the TM^z_{000} (DC) mode. In the presence of the via wall, however, $|E_z|$ is perturbed (with a dip) at the wall location ($\rho = b$), as shown in Figure 2.9. Notice that $|E_z|$ does not completely go to zero at the wall location. Therefore, the dominant mode of the center-fed circular patch is a perturbed TM^z_{000} (DC) mode [63, 64] with the perturbation occurring in the ρ- and ϕ-directions.

2.3.5 Input Impedance and Reflection Coefficient

Full-wave simulation of the center-fed circular patch is performed in HFSS. Figure 2.10 compares the simulated and theoretical input impedance $Z_{in} = R_{in} + jX_{in}$ curves. In the simulation, the patch is fed at the center via with a coaxial TEM field. The theoretical input impedance is calculated using (2.37). The theoretical curves deviate from the simulated curves mainly due to the simplifying assumptions that had to be made in modeling the via wall. There simulated real part R_{in} of Z_{in} is higher than

the theoretical because all the losses have been taken into account in the simulation.

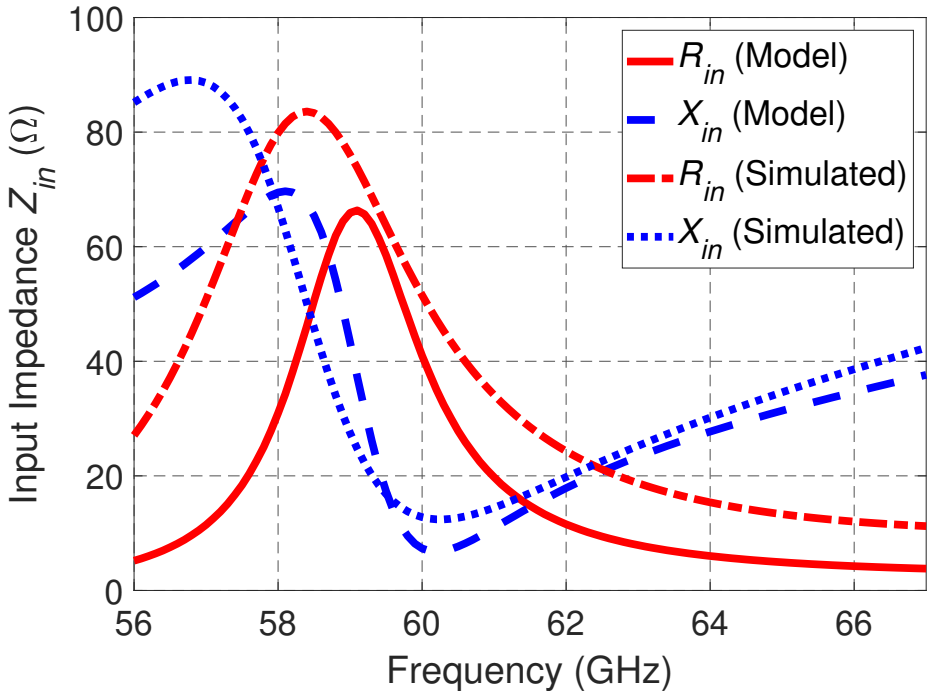


Figure 2.10. Input impedance of the center-fed circular patch with four side vias.

The simulated and theoretical reflection coefficient curves of the center-fed circular patch are shown in Figure 2.11. The theoretical reflection coefficient S_{11} is calculated from the theoretical Z_{in} as follows [24]:

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{2.61}$$

where $Z_0 = 50\ \Omega$ is the characteristic impedance of the transmission line connected at the patch feed. Using the $|S_{11}| \leq -10$ dB criterion, it can be seen that the circular patch has a simulated impedance BW of 2.5 GHz. The cavity model predicts a BW of 1.4 GHz. The deviation is due to the assumption of infinite ground plane when modeling. As the ground plane size is increased, the $|S_{11}|$ decreases and consequently, the BW decreases as well, as will be shown later in Section 2.4.4. A finite ground plane has diffraction at the edges resulting in additional backward radiation. The

Q-factor of the antenna decreases, which increases its BW compared to the antenna (model) with infinite ground plane.

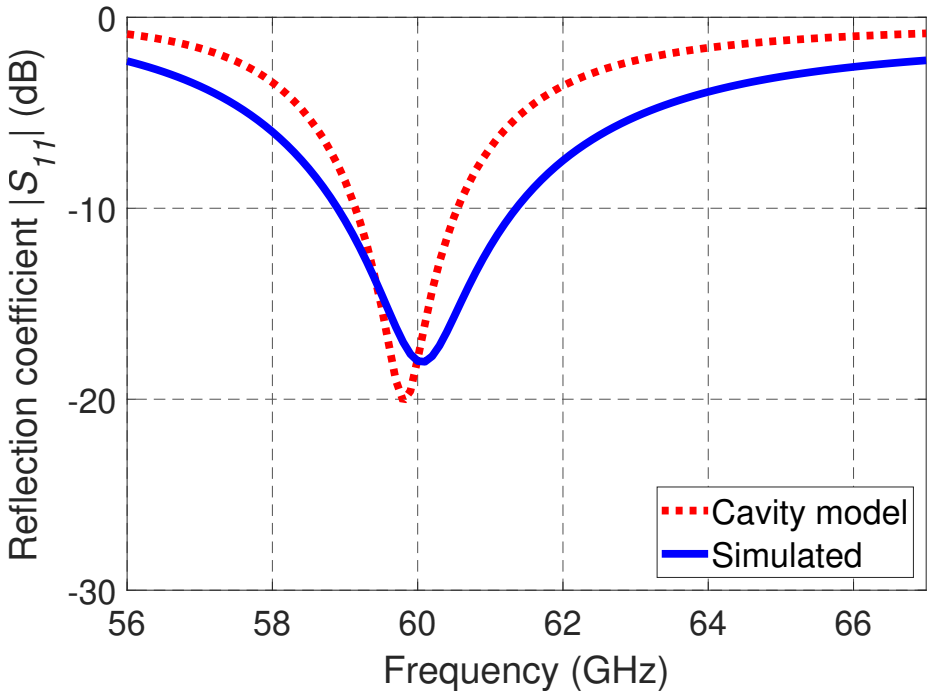


Figure 2.11. Simulated and theoretical reflection coefficient magnitude (dB) of the center-fed circular patch with four side vias.

2.3.6 Radiation Pattern

The radiation pattern characteristics are determined by the dominant mode of the antenna. The perturbed TM^{z}_{000} mode has only small ϕ variation (see Figure 2.9) and no z variation i.e., $n \approx p = 0$ and therefore, the patterns should have monopole-like characteristics. This is verified for the simulated gain patterns of the patch at 60 GHz in the vertical (elevation) and horizontal (azimuth) plane, which are shown in Figure 2.12. Both vertical G_θ and horizontal G_ϕ gain components are shown. From the vertical plane pattern shown in Figure 2.12(a), one can see that the pattern maximum has tilted away from the vertical ($\theta = 0°$). Moreover, the horizontal plane pattern shown in Figure 2.12(b) has azimuthal (ϕ) symmetry within 1 dB and can be

thought of as isotropic in that plane. It is also important to note from the patterns that the patch radiates mostly in G_θ polarization because the z-component of the fringing fields i.e., $|E_z|$ dominates the other components. The vertical pattern in Figure 2.12(a) has no G_ϕ component above the minimum plot scale value of -20 dB. The horizontal pattern in Figure 2.12(b) shows that G_θ polarization is at least 19 dB higher than G_ϕ polarization in the diagonal directions. The highest G_ϕ polarization is 9 dB below G_θ polarization for $W_g = 7.3$ mm.

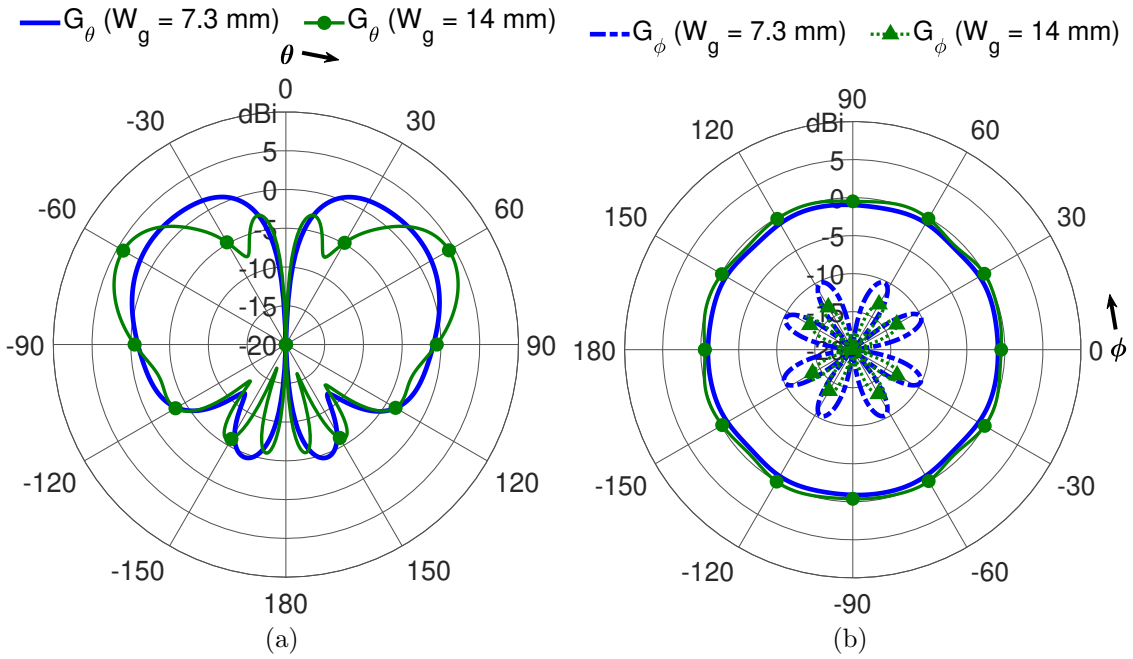


Figure 2.12. Simulated gain patterns (dB) of the center-fed circular patch (with four side vias) at 60 GHz showing both G_θ and G_ϕ gain components for two different ground plane sizes [13]. (a) Vertical plane pattern ($\phi = 0°$). (b) Horizontal plane pattern ($\theta = 90°$).

The ground plane size is increased to 14 mm to see its effect on the radiation pattern of the circular patch. In Figure 2.12(a), one can see that the increase in the ground plane size has further tilted the pattern maximum away from the vertical while producing more ripples in the pattern. The ripples are due to edge diffraction, the nature of which depends on the ground plane size [21]. In the horizontal plane

pattern of Figure 2.12(b), the G_θ component has increased slightly while the G_ϕ component has reduced. Circular ground planes can be used to further reduce the G_ϕ polarization levels [69]. However, the antennas are expected to be mounted on chips that have square or rectangular geometry. A ground plane of similar shape is easier to integrate and also emulates the antenna performance better in the scenario.

2.4 Circular Patch Planar Array

The isotropic elements in Figure 2.1 are replaced by the circular patches to form a 2×2 circular patch planar array. The patch elements are excited with equal amplitude and have the same interelement separation and phase shifts as the isotropic elements they are replacing.

2.4.1 Array Structure

The detailed 3-D structure of the 2×2 circular patch planar array is modeled in HFSS and is shown in Figure 2.13 along with the overlay of simulated 3-D gain pattern (dB) at 60 GHz. The interelement separations, d_x and d_y are both fixed at $d = 1.86$ mm, which corresponds to $d = 0.37\lambda_0$ at wavelength $\lambda_0 = 5$ mm, corresponding to 60 GHz center frequency. This is slightly greater than that given in (2.9) to meet the minimum trace spacing fabrication requirement between the patch edges. The size of the ground plane W_g for the array is kept at 7.3 mm (i.e., same as that for the patch element). Due to mutual coupling, the patch elements in the array do not resonate at 60 GHz when a_f and b are set to the values given in Figure 2.3. The parameter b is optimized to shift the resonant frequency of the patch elements in the array back to 60 GHz. The optimized value of b is 0.67 mm. The important dimensions of the antenna array are summarized in Table 2.3. As shown in Figure 2.13, the main beam of the array is pointed at $\phi_0 = +135^\circ$ as a result of exciting the ports with $\beta_x = +90^\circ$ and

$\beta_y = -90°$ in the simulation, and this matches with what is expected from Table 2.1. It verifies that the array is working as designed.

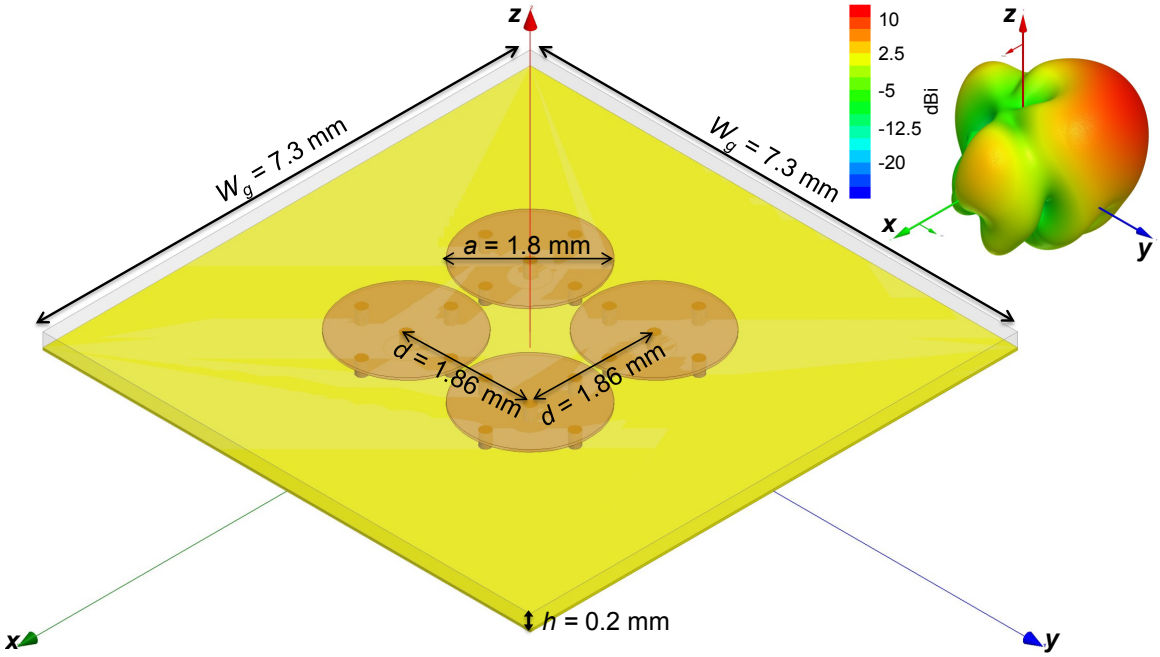


Figure 2.13. 3-D model of 2 × 2 circular patch planar array with simulated 3-D gain pattern (dBi) at 60 GHz. The main beam is pointed at $\phi_0 = +135°$ [13].

Table 2.3. Dimensions associated with the circular patch planar array

Definition	**Dimension**	**Value (mm)**
Diameter of circular patches	a	1.8
Radial distance of side vias	b	0.67
Interelement separation	d	1.86
Core (RO4003C) thickness	h	0.2
Copper thickness	t	0.035
Diameter of center feed vias	a_f	0.15
Diameter of side vias	a_s	0.15
Length/width of the ground plane	W_g	7.3

2.4.2 Switching of Main Beam

The circular patch elements are uniformly excited with interelement phase shifts given in Table 2.1 to scan the main beam of the array in the four diagonal directions. Each combination of phase shifts produces a main beam in one of four diagonal directions. Each element can be excited with a different absolute phase in HFSS. By setting the appropriate absolute phase to each element in the excitation, the required phase difference between elements can be easily realized. The switching of the main beam can be seen in the horizontal gain patterns shown in Figure 2.14, corresponding to four different combinations of β_x and β_y values in Table 2.1.

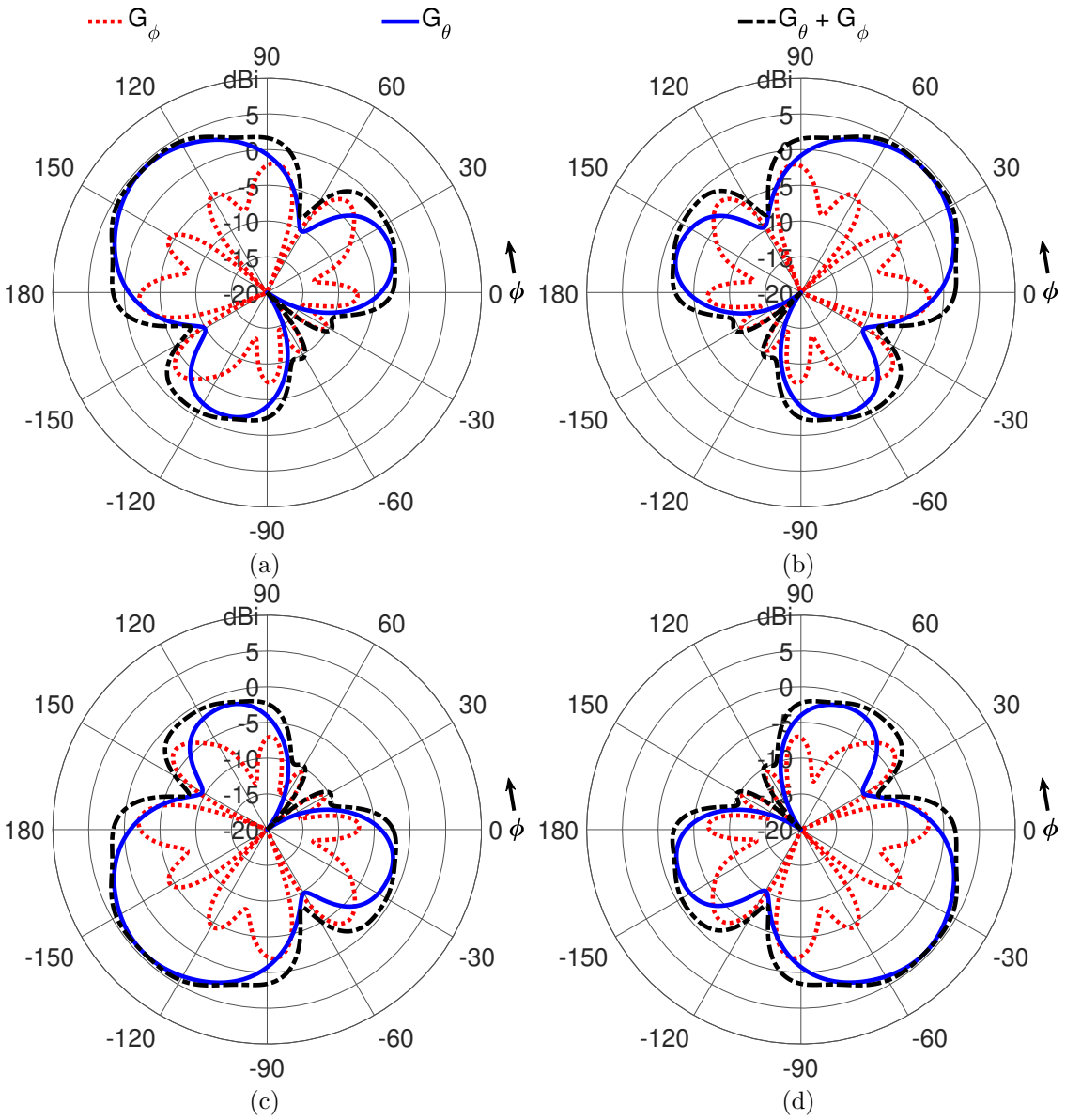


Figure 2.14. Simulated gain patterns (dBi) of the 2 × 2 circular patch planar array at 60 GHz in the horizontal plane ($\theta = 90°$) showing switching of the main beam (for $W_g = 7.3$ mm) [13]. (a) $\phi_0 = +135°$. (b) $\phi_0 = +45°$. (c) $\phi_0 = -135°$. (d) $\phi_0 = -45°$.

The gain patterns show both vertical G_θ and horizontal G_ϕ gain components along with their total ($G_\theta + G_\phi$). The sum represents the total gain in the polarization matched case. Both gain components contribute to the total transmission coefficient when the TX and RX antennas are polarization matched, as will be shown using the

Friis equation in Section 2.5.2. The horizontal patterns represent the horizontal cut of the full 3-D patterns. For example, Figure 2.14(a) is simply the horizontal plane cut of the 3-D gain pattern shown in Figure 2.13. The array has a peak gain of 4.5 dBi at 60 GHz in the horizontal plane. The maximum SLL is 6.1 dB below the peak gain. The array radiates mostly in G_θ polarization (at least 24 dB higher than G_ϕ polarization) along the main beam directions as shown in the radiation patterns of Figure 2.14. This is to be expected since the patch element itself radiates mostly in G_θ polarization (see Figure 2.12). The highest G_ϕ polarization of the array is 7 dB below the peak gain. Increasing the size of the ground plane to 14 mm increased the peak gain of the array to 5.75 dBi while reducing the highest G_ϕ polarization to 12 dB below the peak gain. This is again expected since a similar trend is observed in the radiation pattern of the isolated patch element (see Figure 2.12) when the ground plane size is increased.

2.4.3 SLL reduction

When mutual coupling is ignored, the SLLs can be 10 dB below the peak for a uniformly excited 2×2 planar array of isotropic elements, as is shown in Section 2.2.2. The simulated pattern, shown in Figure 2.14, has much higher SLLs attributable to the presence of mutual coupling between the patches. Since mutual coupling cannot be avoided when array elements are close to one another, other methods must be used for SLL reduction. One such method is to taper the amplitude distribution at the array feed [21]. About 1.3 dB reduction in SLL and deeper nulls are achieved for G_θ polarization when half-power taper is applied, as shown in the simulated patterns in Figure 2.15. The amplitude distribution is shown in Table 2.4 for half-power and uniform cases. The peak gain has increased slightly because of the taper. Reducing the SLLs can consequently reduce the unwanted radiation and reduce cross-talk and interference.

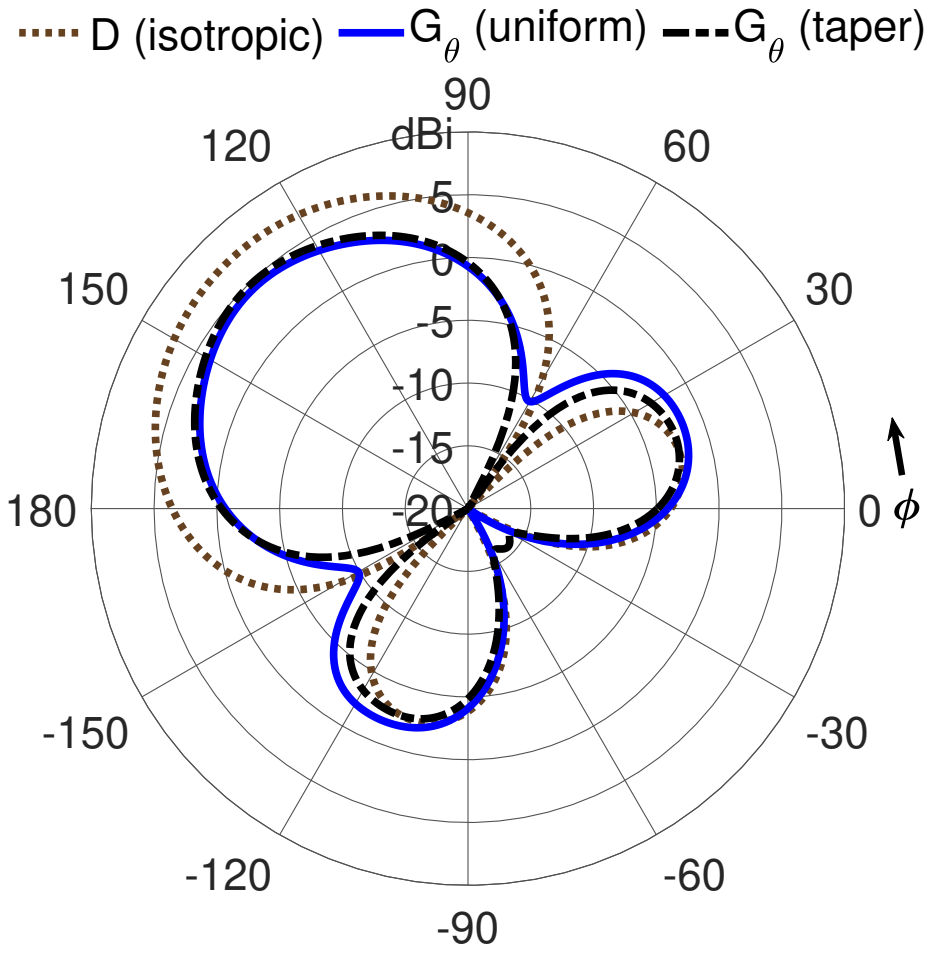


Figure 2.15. SLL reduction by tapering the element amplitude excitation of the array.

Table 2.4. Array feed distribution without and with taper

Array	**Element Feed Amplitude**	**Peak Gain**	**SLL**
Isotropic	Uniform: $\|a_1\| = \|a_2\| = \|a_3\| = \|a_4\| = 1$	7.41 dBi	10 dB
Patch	Uniform: $\|a_1\| = \|a_2\| = \|a_3\| = \|a_4\| = 1$	4.5 dBi	6.1 dB
Patch	Half-Power: $\|a_1\| = 1, \|a_2\| = \|a_3\| = 0.71, \|a_4\| = 0.5$	4.9 dBi	7.37 dB

2.4.4 Reflection Coefficient

A center-fed circular patch by itself has poor return loss because the electric field value vanishes at the center [21]. The side vias change the boundary condition at the

patch center and allow much better return loss with a center feed [60, 61]. Since the patches are so close to one another, the near-field coupling between them also affects the input impedance. This mutual coupling effect is automatically taken into account in the full-wave simulation. In the presence of mutual coupling, the optimized value of $b = 0.67$ mm makes the patch elements in the array resonate at 60 GHz. Figure 2.16 shows the optimized reflection coefficient (in blue solid) of the circular patch elements in the array, obtained from simulation. All the elements have identical reflection coefficients since each element is identically coupled to the others. An impedance BW of 5.6 GHz is achieved, using the $|S_{11}| \leq -10$ dB criterion, around the 60 GHz when $a_f = 0.15$ mm, $b = 0.67$ mm, and $W_g = 7.3$ mm.

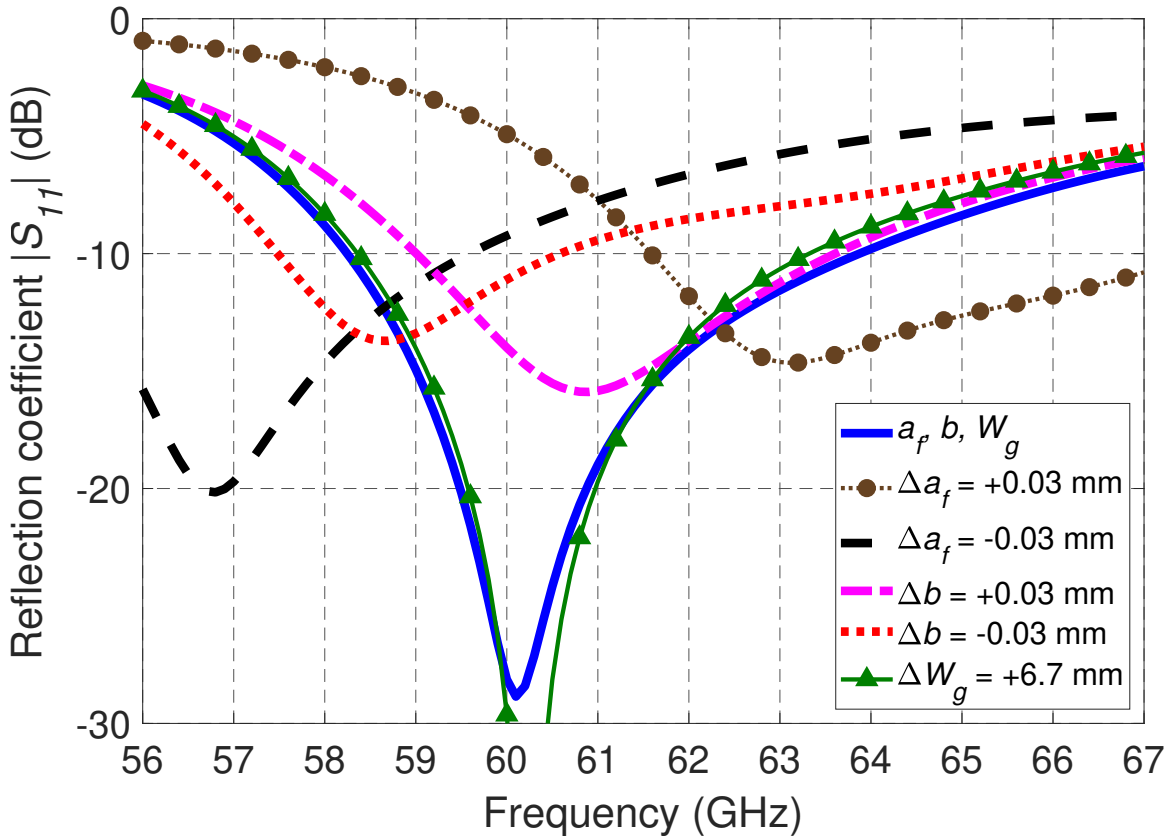


Figure 2.16. Reflection coefficient magnitude (dB) of the center-fed circular patch elements in the 2 × 2 array [13].

Figure 2.16 also shows how the reflection coefficient of the circular patch elements in the array changes with variations in the parameters a_f, b, and W_g. Only one parameter is varied at a time while the other two are kept at their original values given in Figure 2.3. The resonant frequency (f_0), reflection coefficient magnitude ($|S_{11}|$) and impedance BW are most sensitive to the changes in a_f. Due to a large shift in the resonant frequency, the $|S_{11}|$ at 60 GHz has gone above -10 dB and the BW cannot be defined for $\Delta a_f = \pm 0.03$ mm. Therefore, this parameter should have tight tolerances for fabrication. The performance of the array has moderate sensitivity to the changes in b, whereas little sensitivity to the increase in W_g. The larger ground plane did help to improve (reduce) the $|S_{11}|$ at 60 GHz but with a slight reduction in BW. The performance changes are summarized in Table 2.5.

Table 2.5. Sensitivity of array performance to changes in antenna parameters [13]

Parameter Deviation[a]		**Array Performance**		
		f_0	$\|S_{11}\|$ (at 60 GHz)	BW ($\|S_{11}\| \leq -10$ dB)
Δa_f	+0.03 mm	63.1 GHz	−4.9 dB	N/A
	−0.03 mm	56.8 GHz	−9.2 dB	N/A
Δb	+0.03 mm	60.9 GHz	−14 dB	4.5 GHz
	−0.03 mm	58.7 GHz	−11.1 dB	3 GHz
ΔW_g	+6.7 mm	60.2 GHz	−29.6 dB	4.9 GHz

[a] Deviations are changes from the original parameter values: $a_f = 0.15$ mm, $b = 0.67$ mm, and $W_g = 7.3$ mm.

2.4.5 Antenna Packaging Considerations

The array achieved a simulated radiation efficiency of 97% at 60 GHz. This high efficiency is attributed mainly to the use of the low-loss RO4003C substrate. An AiP implementation of the proposed array is intended for integration with the CMOS chip. The AiP solution is recommended [28] because it offers lower loss and thus

better signal-to-noise ratio (SNR) over an AoC implementation in lossy silicon [27], as is discussed in Section 1.10. Before the antenna can be packaged with the chip, the feed network that attains the required interelement phase shifts must be realized on a separate layer below the ground plane as depicted in Figure 2.17. The presence of the feed network will change how the array performs, overall, which is analyzed in detail in Chapter 3. Nonetheless, the array performance without the feed network is a useful baseline for comparison when the feed network is eventually integrated to form the antenna module. The module can then be connected to the CMOS chip by using solder balls/bumps [28, 34]. One cost-effective way to do this is to use the solder balls to connect the feed layer with the chip package mounted on the printed circuit board (PCB), as shown in Figure 2.17. Another possibility is to directly connect the antenna to the CMOS die using solder bumps with die-attach methods, which is a faster performing integrated solution. The solid ground plane helps to minimize interference by blocking antenna radiation into the feed and the CMOS circuits underneath and vice-versa.

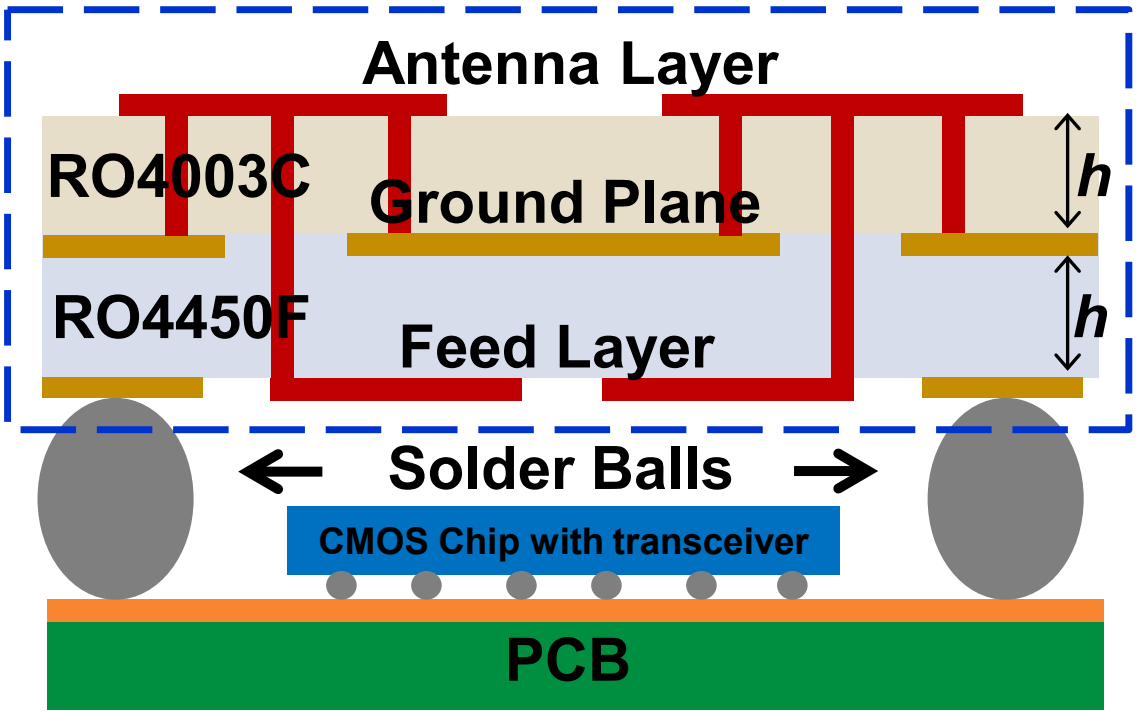


Figure 2.17. Illustrative side view of the antenna structure showing antenna, ground, and feed layers in AiP implementation. The antenna module is shown as mounted over a CMOS chip using solder balls.

2.4.6 Antenna Substrate Considerations

Rogers RO4003C laminate is chosen as the antenna substrate because it has low dielectric loss, and unlike polytetrafluoroethylene (PTFE) based laminates, it does not require any additional chemical wetting preparation process for plated-through hole (PTH) via formation. Since each patch element has multiple vias, the use of RO4003C laminates can greatly simplify the fabrication of the antenna array. Moreover, as shown in Figure 2.17, RO4003C laminates can be stacked and bonded with RO4450F bondplys following standard PCB fabrication techniques to realize a cost-effective multilayer structure [62].

2.5 Friis Equation and Polarization Considerations in Inter-chip Communication

The Friis transmission equation can be used to get a general idea of how the polarization components of the chip-to-chip antennas affect link transmission.

2.5.1 Far-Field Criteria

The Friis equation is valid if the antennas are in the far-field regions of one another. For an antenna array, the far-field criteria [21] are satisfied at a distance R from the center of the array if

$$R \gg \lambda_0 \tag{2.62}$$

and

$$R \geq \frac{2D^2}{\lambda_0} \tag{2.63}$$

where D is the largest dimension of the array. For broadband antennas, the criterion in (2.63) must be satisfied for all wavelengths (frequencies) within the antenna BW for accurate modeling of the wireless link. For the 2×2 circular patch planar array shown in Figure 2.13, the largest dimension is the diagonal length of the array i.e., $D = 4.5$ mm and the far-field criterion in (2.63) is satisfied for $R \geq 7.78$ mm at 60 GHz. The criterion is most restrictive for the highest frequency $f_{\max}$ (corresponding to the smallest wavelength $\lambda_{\min}$) considered. If the criterion is satisfied at $f_{\max}$, it will be satisfied at any frequency lower than $f_{\max}$ i.e., $f \leq f_{\max}$ (corresponding to $\lambda_0 \geq \lambda_{\min}$ in (2.63)). Since the highest measurement frequency is $f_{\max} = 67$ GHz in this dissertation, the far-field criterion is satisfied at all frequencies $f \leq 67$ GHz if the antenna arrays are separated by $R \geq 9$ mm. This far-field criterion is easily satisfied for typical chip-to-chip distances at few tens of millimeters [53]. However, the criterion in (2.62) is only loosely satisfied for $5.4 \geq \lambda_0 \geq 4.5$ mm (i.e., $56 \leq f \leq 67$ GHz), which indicates that there will be some residual near-field effects at the distances

considered. Therefore, the Friis equation cannot quantitatively model the chip-to-chip link at those distances. The field behavior associated with the near-field is ignored. Moreover, the power decay behavior along the air-dielectric interface is different [60] from the $1/R^2$ behavior present in the Friis equation [21]. Nevertheless, the Friis equation can provide a qualitative understanding of how the gains and the polarization components of the TX and RX antennas affect the link transmission. A more accurate link model that considers the field behavior at the interface is presented in Chapter 4.

2.5.2 Frequency-Dependent Friis Equation With Polarization

To account for frequency variations and polarization, the frequency-dependent reflection coefficient, and the antenna gain components are used in the Friis equation as follows [70]:

$$\frac{P_r}{P_t} = \left(1 - |S_{11}(f)|^2\right)^2 \left(\frac{\lambda_0}{4\pi R}\right)^2 G_{TX}(f, \theta_t, \phi_t) G_{RX}(f, \theta_r, \phi_r) \text{PLF} \tag{2.64}$$

where $S_{11}(f)$ represents the frequency-dependent reflection coefficient of the identical TX and RX antennas, PLF is the polarization loss factor, and $G_{TX}(f, \theta_t, \phi_t)$ and $G_{RX}(f, \theta_r, \phi_r)$ are the frequency- and angle-dependent gains of the TX and RX antennas, respectively, along the LoS. $G_{TX}(f, \theta_t, \phi_t)$ and $G_{RX}(f, \theta_r, \phi_r)$ can be same or different even for identical TX and RX antennas depending on their orientation $(\theta_t,\ \phi_t)$ and $(\theta_r,\ \phi_r)$ with respect to the LoS. The other parameters are defined in Section 1.9.1. The switchable nature of the antennas means that the gains are also the functions of the pattern configuration (see Figure 2.14). The received power P_r represents the signal power S when the RX antenna is receiving from an intended TX and interference power I when the RX antenna is receiving from an unintended TX. The PLF is defined as

$$\text{PLF} = |\cos \psi_p|^2 \tag{2.65}$$

where ψ_p is the angle between the electric field vectors $\vec{E}_{TX}$ and $\vec{E}_{RX}$ of the TX and RX antennas, respectively. They can be decomposed into the vertical E_θ and the horizontal E_ϕ polarization components as follows:

$$\vec{E}_{TX}(f,\theta_t,\phi_t) = E_{\theta_t}(f,\theta_t,\phi_t)\hat{a}_\theta + E_{\phi_t}(f,\theta_t,\phi_t)\hat{a}_\phi \tag{2.66}$$

$$\vec{E}_{RX}(f,\theta_r,\phi_r) = E_{\theta_r}(f,\theta_r,\phi_r)\hat{a}_\theta + E_{\phi_r}(f,\theta_r,\phi_r)\hat{a}_\phi \tag{2.67}$$

The gains of the TX and RX antennas can also be decomposed into the vertical G_θ and the horizontal G_ϕ polarization components as follows:

$$G_{TX}(f,\theta_t,\phi_t) = G_{\theta_t}(f,\theta_t,\phi_t) + G_{\phi_t}(f,\theta_t,\phi_t) \tag{2.68}$$

$$G_{RX}(f,\theta_r,\phi_r) = G_{\theta_r}(f,\theta_r,\phi_r) + G_{\phi_r}(f,\theta_r,\phi_r) \tag{2.69}$$

The gain components G_θ and G_ϕ are related to their respective electric field components E_θ and E_ϕ of the antennas as follows [21]:

$$G_{\theta,\phi} = \frac{2\pi}{\eta_0 P_t}|E_{\theta,\phi}|^2 \tag{2.70}$$

where $\eta_0 = 377\ \Omega$ is the intrinsic impedance of free-space.

Each reflection loss term $(1-|S_{11}(f)|^2)$ in (2.64) can be combined into a gain term $G_{\theta,\phi}$ and the product is called the realized gain $G_{\theta,\phi(\text{rlzd})}$, expressed as

$$G_{\theta,\phi(\text{rlzd})} = (1-|S_{11}(f)|^2)G_{\theta,\phi} \tag{2.71}$$

In order to see how polarization affects transmission, two scenarios can be considered. If the main beams of the TX and RX arrays are pointed at one another such that $E_{\theta_t}/E_{\phi_t} = E_{\theta_r}/E_{\phi_r}$, then PLF = 1 in (2.65) since $E_{\theta_t} = E_{\theta_r}$ and $E_{\phi_t} = E_{\phi_r}$ and $\psi_p = 0$. Also, $G_{\theta_t} = G_{\theta_r}$ and $G_{\phi_t} = G_{\phi_r}$ and using (2.68) and (2.69) in (2.64) with the aforementioned substitutions, the factor $G_{TX}(f,\theta_t,\phi_t)G_{RX}(f,\theta_r,\phi_r)$ simplifies to $(G_{\theta_t}+G_{\phi_t})^2$ in (2.64), and thus both gain components add to the total transmission. The radiation coupling is maximized due to main beams pointing at one another

with PLF = 1. On the other hand, if the beam configuration of the arrays is such that $E_{\theta_t}/E_{\phi_t} \neq E_{\theta_r}/E_{\phi_r}$, then some polarization mismatch will occur (i.e., PLF $<$ 1) since $\psi_p > 0$. This can actually be desirable when unwanted radiation coupling (interference) between the arrays is to be reduced. When the patterns are switched, the direction of polarization components can change, and the link budget can vary due to the change in PLF. Therefore, care must be taken to account for the antenna polarization components when patterns are reconfigured.

Chapter 3
2-D Butler Matrix and Its Integration With the Array

A 2-D Butler matrix feed network is designed, implemented, and integrated with the 60-GHz 2×2 circular patch planar array. Some of the contents of this chapter have been published in [14]. This chapter is also a part of the patent application in [71]. The realized antenna module is a thin multilayer MS structure with a footprint smaller than that of a typical multicore chip. Therefore, the module can be packaged with the chip with minimal area overhead. The matrix's inputs can be individually excited to easily scan the array main beam in the four diagonal directions. The antenna module thus provides a seamless and practical way to achieve reconfigurable interchip communication in MCMC systems.

3.1 Introduction

Reconfigurable interchip communication in MCMC computing systems can be achieved through the use of mmW switched-beam antenna arrays connected to CMOS chip routers [13, 71]. Traditionally, the mmW antennas have been used to provide high-speed wireless interconnection between the chips to solve the wiring complexity problem in such systems [8, 10–12, 41]. The wireless interconnects require the use of transceivers and beamforming networks (BFNs) along with the antennas for data transfer [8,10]. Beamforming using solid-state phase shifters is not practical at mmW frequencies due to high loss [72]. Pattern reconfiguration at 60 GHz by simply switching array elements ON and OFF has been proposed in [42]. The loss in the switch network will depend largely on the type and number of switches used [73, 74]. For example, using just one single-pole n-throw (SPnT) switch to feed the array elements can minimize the loss. But this also means only one element can be fed at a time,

resulting in lower directivity and gain. Alternatively, the Butler matrix and the Rotman lens have been extensively used as BFNs for linear arrays at 60 GHz [59, 75–79]. One advantage of using BFNs is that all the elements in the array can be fed simultaneously to get high directivity, with relatively small footprint. There are, however, increased losses in the BFN. The BFN footprint will also increase the antenna module size. The BFNs still require one SPnT switch at the front end, which contributes to additional losses.

The scan coverage of an array is determined by the type of the array used [58]. A linear array is capable of only 180° scan coverage when using the traditional one-dimensional (1-D) Butler matrix [75]. On the other hand, a planar array can be fed by the 2-D Butler matrix, which is a combination of two 1-D Butler matrices. The inputs of the 2-D matrix are isolated from one another and the power is equally divided at the outputs. Thus, the 2-D Butler matrix retains the properties of the 1-D Butler matrix. In [56], an eight-beam endfire scanning array using magneto-electric (ME) dipole elements with the 1-D Butler matrix has been demonstrated but the angular coverage is limited to 180°. A BFN based on the 1-D Butler matrix with stacked-patches that scans in two planes is presented in [50] but for broadside scanning. A substrate integrated waveguide (SIW) implementation of the 2-D Butler matrix with a ME dipole planar array is presented in [57], but also for broadside scanning.

In this chapter, the 60 GHz circular patch planar arrays with integrated 2-D Butler matrices provide both the space and surface wave interconnection. The antenna modules have four diagonal endfire beams with significant surface wave excitation, which helps to increase the power coupling between the chips and improve signal power at large distances. The type and implementation of the antenna feed network chosen will determine the ease with which the array can be connected with the integrated CMOS transceivers on the chips. A MS implementation of the 2-D Butler matrix is pursued due to the simplicity in fabrication and eventual integration with the array.

3.2 HSSW-I

Besides the broad BW, the 60 GHz operating frequency offers several other advantages. The atmospheric absorption near 60 GHz provides higher interference suppression at long range that reduces off-system interference to neighboring devices [23]. In addition, the transceivers already developed for 60 GHz WLAN applications [20] and compliant with IEEE 802.11ad and 802.11ay standards can be utilized for multi-Gbps data rates, as discussed previously in Sections 1.7 and 1.12. The antenna array and feed network at 60 GHz can be made small enough to fit over a multicore chip of a typical size [53] with little to no area overhead and ultimately minimize the chip-to-chip distances, as illustrated in Figure 3.1. The arrays must provide communication over these distances, usually several tens of millimeters, as dictated by the chip/antenna size. Figure 3.2 shows how the antenna module can be packaged (surface mounted) over the CMOS chips (which has integrated transceivers and multiple cores). The chips are ball grid array (BGA) mounted on the board. Another option is to use a double-sided PCB board to mount the antenna modules. By matching the layout and arrangement of the antenna modules to the chips underneath, the substrates and ground planes of each antenna module can be connected together to form a HSSW-I layer parallel to the PCB board/chips and thus take advantage of the surface wave coupling in addition to the space wave coupling. The microwave monolithic integrated circuit (MMIC) SPnT switch can be flip-chip (C4) attached to the feed layer. The transceivers serialize/deserialize the data to be exchanged and provide the 60 GHz modulated/demodulated signals for transmission/reception by the antennas [20]. This will minimize the number of connections required between the chip and antenna module [10, 20]. The PCB board is needed for providing power to the chips and for auxiliary communications with other system components.

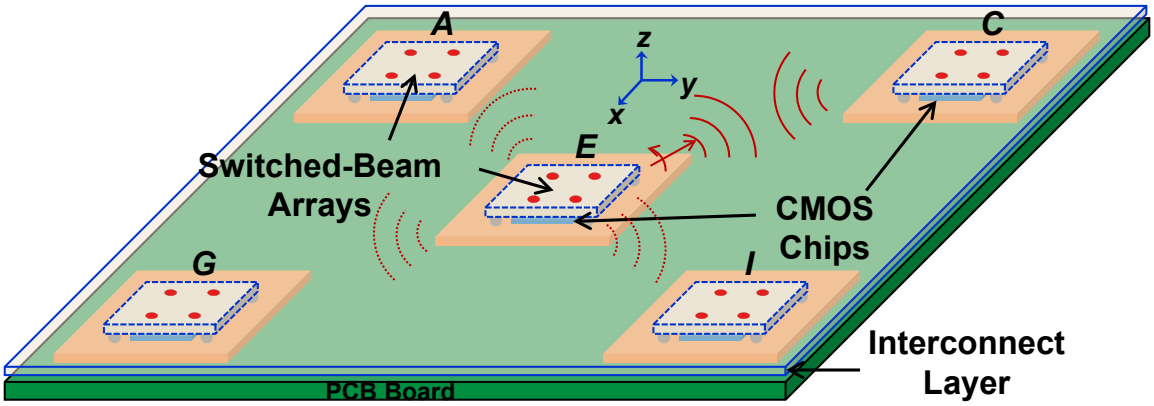


Figure 3.1. The antenna modules are packaged on top of multicore CMOS chips. The antenna arrays provide switchable beams in the horizontal plane for reconfigurable chip-to-chip communications [14].

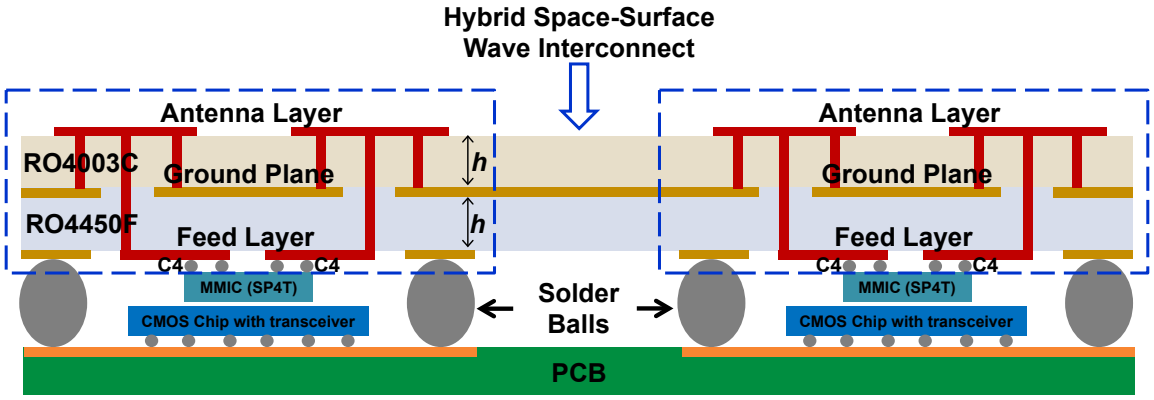


Figure 3.2. Detailed side view of Figure 3.1 showing the HSSW-I for 60-GHz chip-to-chip communications. The multilayer antenna modules are surface mounted on the PCB board over the chips [14, 71].

Figures 1.8, 3.1 and 3.2 depict how the antenna arrays can be used for interchip communication [13, 71]. The cores on a chip communicate through short high speed wired links whereas long distance communication between chips is done through the HSSW-I layer using the planar arrays. Note that in order for a module (e.g., E in Figure 3.1) to communicate to all its eight adjacent neighbors (only four shown), the array should provide eight beams, as illustrated in Figure 1.8. A planar array with more than four elements may be necessary to get the eight beams. A simpler case

of beam scanning in only the diagonal directions with four beams is demonstrated in this dissertation. Interchip communication in the diagonal directions can reduce the average hop count and latency in the network [19]. In the MCMC system of Figure 3.1, the antenna arrays all lie in the same xy-plane, and hence, they must be capable of in-plane endfire scanning. Therefore, MCMC systems present a unique challenge of endfire scanning with 360° angular coverage on the design of the antenna arrays.

3.3 2-D Butler Matrix for Planar Array

3.3.1 Working Principle of 2-D Butler Matrix

The four-input, four-output (4×4) 2-D Butler matrix with a 2×2 planar array is shown in Figure 3.3. It provides four switchable diagonal beams in the azimuth plane (endfire). As illustrated in Figure 3.3, the proposed 2-D Butler matrix must still be augmented with a MMIC single-pole four-throw (SP4T) switch at its input to enable electronic feed line switching [78]. The main beam direction of the array is determined by the input selected. The control switch must have attributes such as low loss, low bias and drive voltage, high isolation, high switching speed, and good reliability. Electronic switches in the form of microelectromechanical systems (MEMS) [72], PIN diodes, and field-effect transistors (FETs) [78] have been used for line switching at 60 GHz.

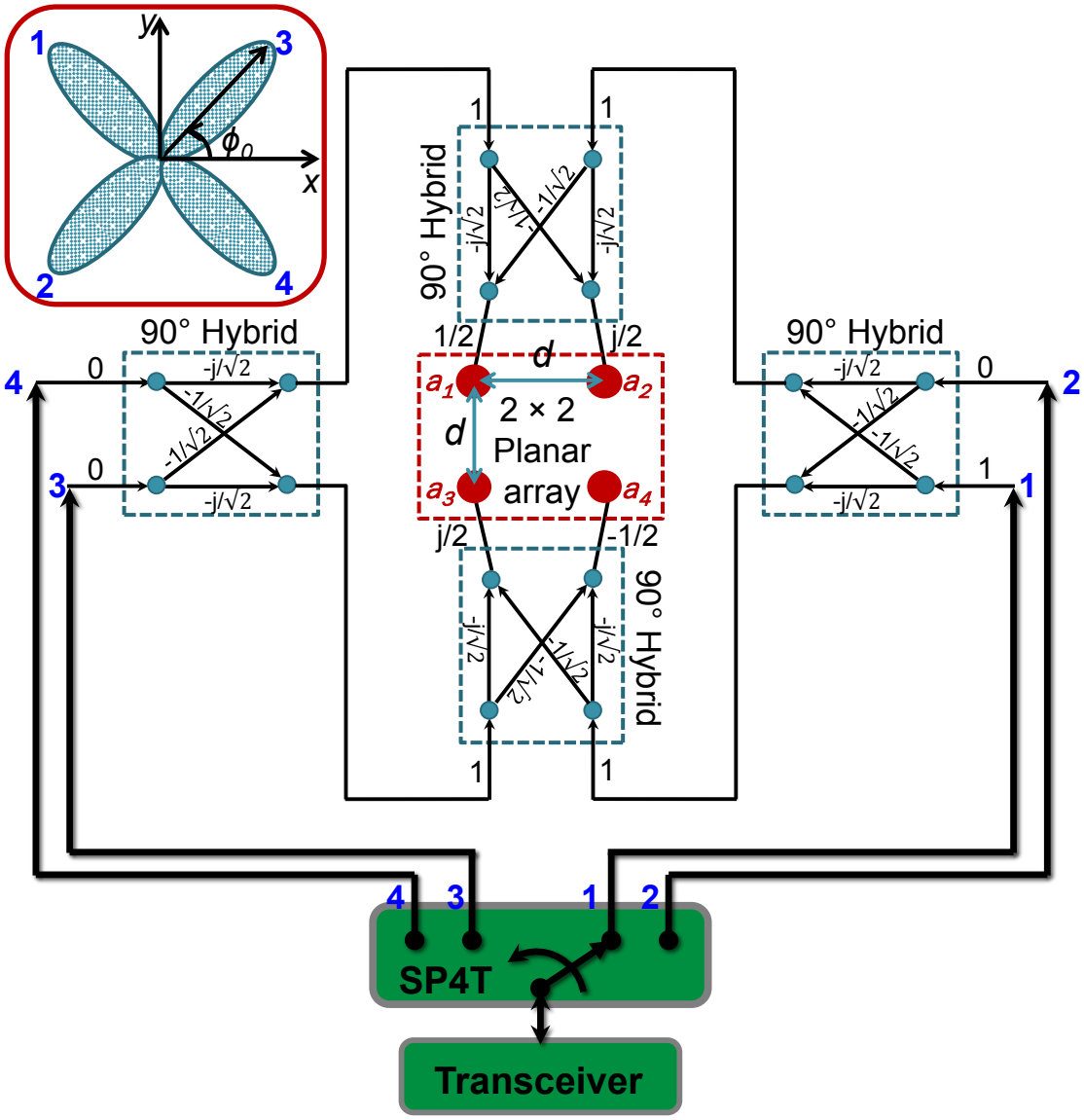


Figure 3.3. 4 × 4 2-D Butler matrix for planar array (360° angular coverage in 90° steps). The SP4T switch enables electronic scanning of the array main beam by connecting one of the Butler matrix inputs to the transceiver [14, 71].

The 4 × 4 2-D Butler matrix consists of four quadrature (90°) hybrid couplers interconnected to provide a specific phase difference between the output signals (connected to the array feed) for each input excitation. The interelement phase shifts obtained at the array feed by exciting each of the four input ports are listed in Ta-

ble 3.1.

Table 3.1. Interelement phase shifts and main beam direction attained for each input port excitation of the Butler matrix [13, 14, 71]

Port	$\boldsymbol{\phi_0}$	$\boldsymbol{\beta_x}$	$\boldsymbol{\beta_y}$
1	$+135°$	$+90°$	$-90°$
2	$-135°$	$+90°$	$+90°$
3	$+45°$	$-90°$	$-90°$
4	$-45°$	$-90°$	$+90°$

The four output ports are arranged in a 2×2 grid format to match the layout of the planar array and realize the $\pm 90°$ phase difference in both the x- and y-directions. In order to understand how the proposed matrix in Figure 3.3 attains the required phase shifts in Table 3.1, the case for port 1 excitation is considered. Figure 3.3 shows the signal flow graph. For port 1 excitation, the two arms of the right coupler produce signals $-j/\sqrt{2}$ and $-1/\sqrt{2}$ at the coupler output. The signal $-j/\sqrt{2}$ from the bottom arm is further split by the bottom coupler into signals $-1/2$ at a_4 and $j/2$ at a_3 while the signal $-1/\sqrt{2}$ from the top arm is further split by the top coupler into signals $j/2$ at a_2 and $1/2$ at a_1. This effectively achieves $\beta_x = +90°$ and $\beta_y = -90°$ and produces the main beam along $\phi_0 = +135°$ (see Table 3.1). Each input port is isolated from the other and there is equal power division at the output ports.

Note that the proposed matrix does not require the use of crossovers and $45°$ phase shifters, unlike that of the 4×4 1-D Butler matrix shown in Figure 3.4.

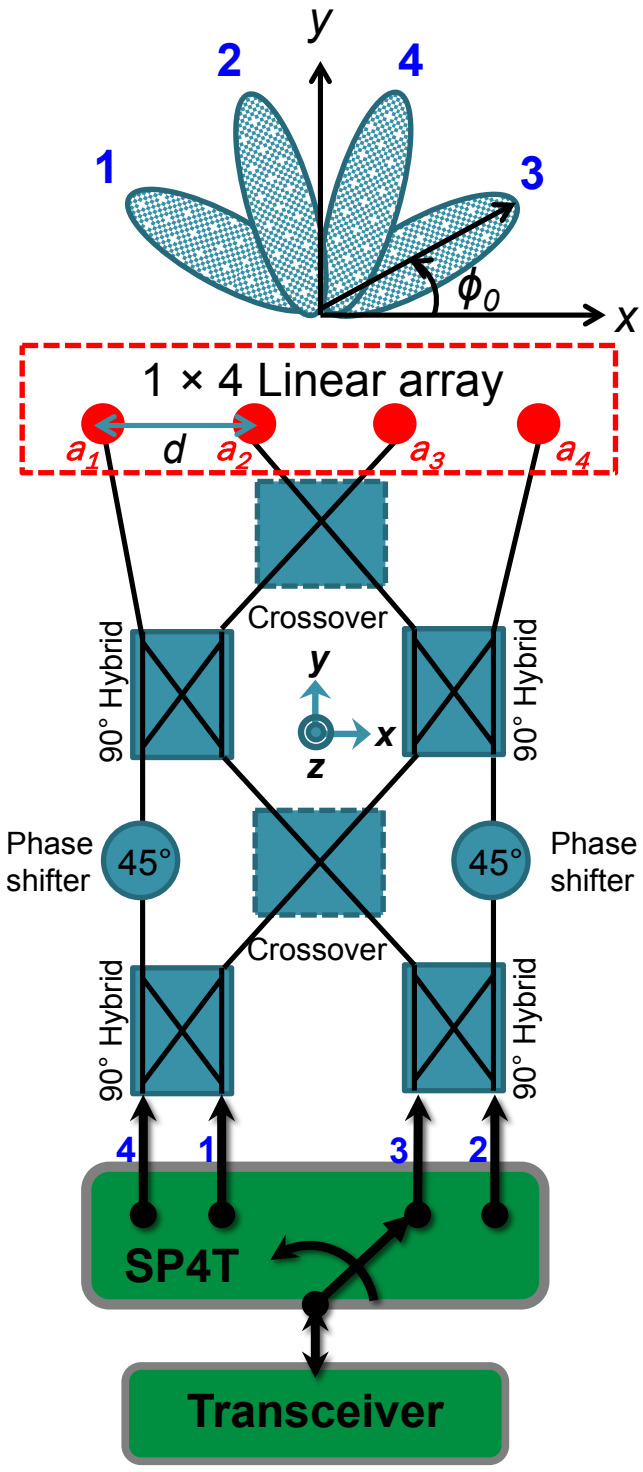


Figure 3.4. 4 × 4 1-D Butler matrix for linear array (only 180° angular coverage) [59].

3.3.2 MS Quadrature (90°) Hybrids

The 90° hybrids shown in Figure 3.3 must first be designed and characterized to realize the 4 × 4 2-D Butler matrix. The hybrids are implemented in MS form for ease of fabrication and measurement. The hybrids are printed on a Rogers RO4450F prepreg ($\epsilon_{r,p} = 3.52, \tan\delta_p = 0.004$) [80] of height $h = 0.2$ mm, as a part of the feed layer of the stackup shown in Figure 3.2. The prepreg is a bonding layer that is required to create multilayer structures with the RO4003C core. Figure 3.5(a) shows a MS 90° hybrid that is designed and modeled in HFSS. The simulated S-parameters are shown in Figure 3.5(b) and the output phase difference is shown is Figure 3.5(c).

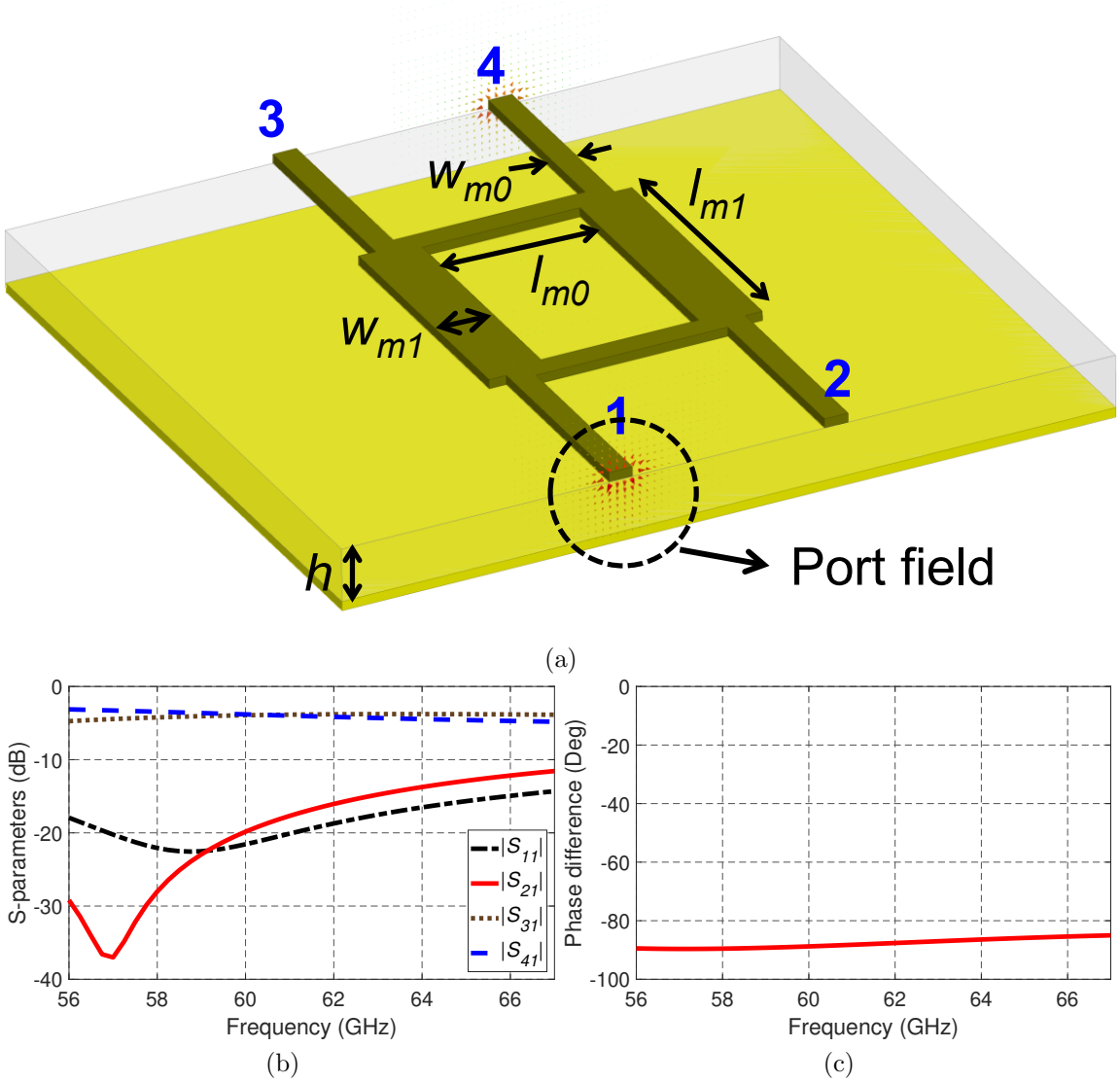


Figure 3.5. MS quadrature (90°) hybrid. (a) 3-D model showing port field at 60 GHz. (b) Simulated S-parameters. (c) Phase difference between the output ports 4 and 3.

At the design frequency, assuming single-mode operation, the magnitude and phase relationship of the signals at and between all the four ports of a lossless 90° hybrid can be expressed in the S-matrix form as follows [24]:

$$[S_Q] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ 0 & 1 & j & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \end{bmatrix} \tag{3.1}$$

At 60 GHz in Figure 3.5(b), the power is nearly equally divided (near 3-dB) at the output ports. And, in Figure 3.5(c), there is about -90° phase difference between the output ports. The ports 1 and 2 are isolated. Therefore, the simulated S-parameters closely follow the relationship given in (3.1). The nature of the port field at 1, as shown in Figure 3.5(a), indicates that the quasi-TEM MS mode is excited in the structure verifying the single-mode operation. The performance of the MS hybrid is limited by the coupling of the fields between its arms. The dimensions of the hybrid are given in Table 3.2.

Table 3.2. Dimensions associated with the Butler matrix: 90° hybrid and quarter-wave line (QWL)

Definition	**Dimension**	**Value (mm)**
Prepreg (RO4450F) thickness	h	0.2
Copper thickness	t	0.035
Width of 100 Ω MS line	w_{m0}	0.09
Width of 70.7 Ω MS line and QWL	w_{m1}	0.22
Width of 50 Ω MS line	w_{m2}	0.45
Length of 100 Ω MS line	l_{m0}	0.73
Length of 70.7 Ω MS line	l_{m1}	0.98
Length of 70.7 Ω QWL	l_q	0.89
Inter-coupler distance	l_c	8.11

3.3.3 Implementation of Butler Matrix

A total of four hybrids [identical to the one shown in Figure 3.5(a)] are interconnected and arranged, like in Figure 3.3, to realize the Butler matrix. The matrix is realized as a feed layer on a Rogers RO4450F prepreg, as illustrated in Figure 3.2. The middle ground plane helps to minimize interference by blocking antenna radiation into the feed layer and CMOS circuits underneath. The 3-D model of the Butler matrix created in HFSS is shown in Figure 3.6. The feed layer resides below the ground plane (hidden). On the given prepreg, the 50 Ω lines are too wide at 60 GHz to realize the hybrids with sufficient separation between their arms and achieve good performance.

Therefore, the narrower 100 Ω MS lines are used to realize the hybrids [59]. The input and output ports are labeled in Figure 3.6 and have impedances of 100 and 50 Ω, respectively. The input ports $i = 1$ to 4 must be later transformed to 50 Ω for probing (see Section 3.4). The inter-coupler distance l_c is set so that it is long enough to interconnect the hybrids under the given layout and routing constraints. With $l_c = 8.11$ mm, there is sufficient separation between the neighboring lines so that they do not couple with one another. This length can be conveniently set without affecting the phase difference at the matrix output. The key dimensions of the Butler matrix are labeled in Figure 3.6 and their values are listed in Table 3.2.

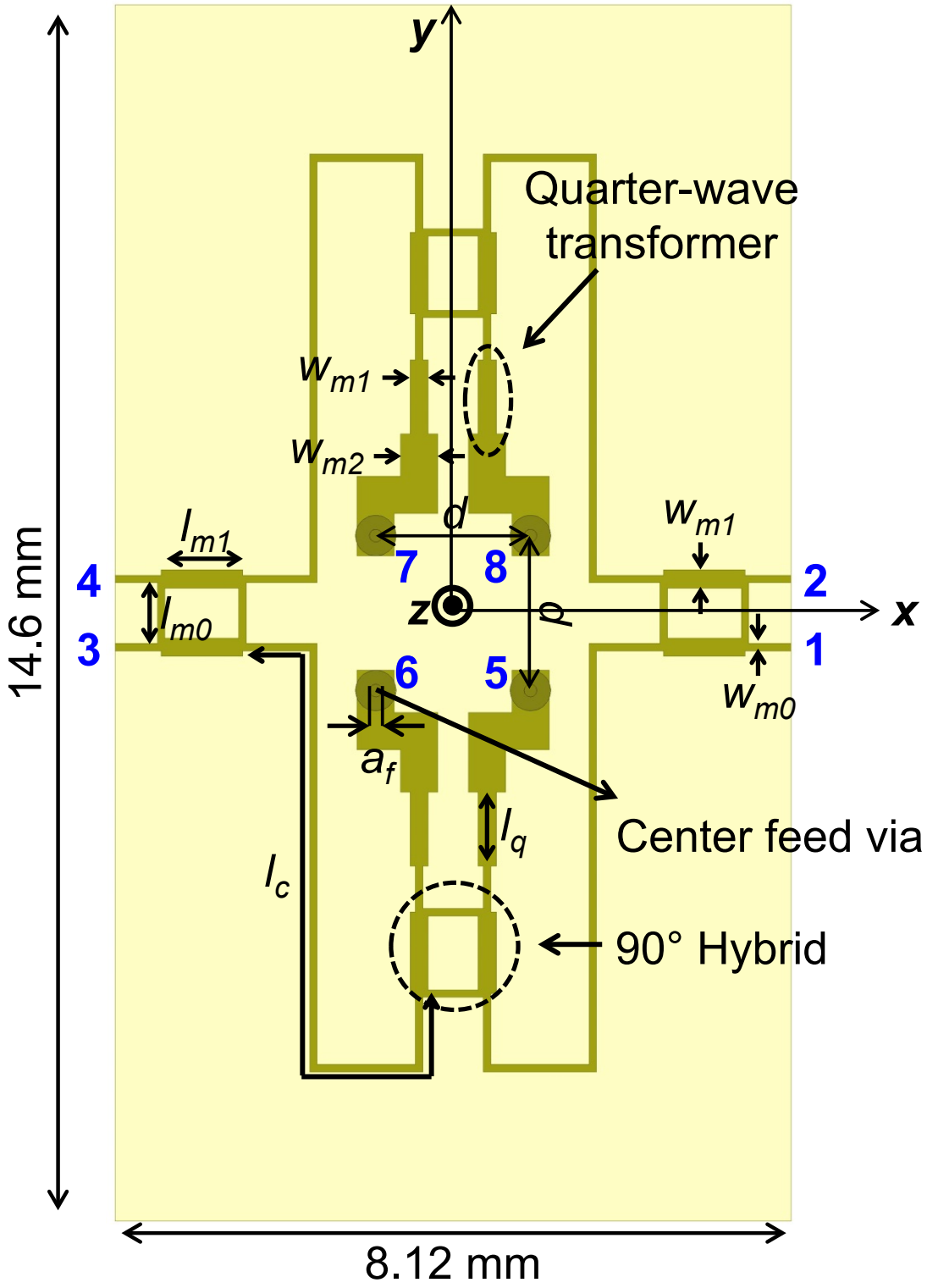
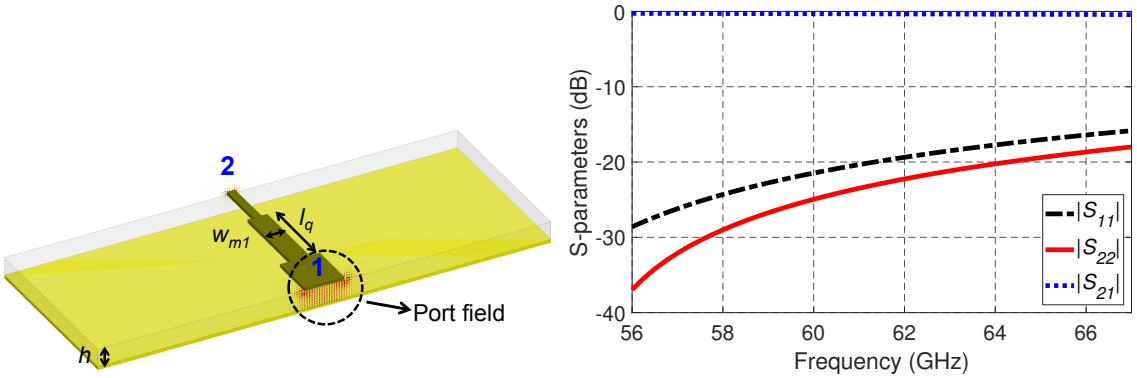


Figure 3.6. 3-D model of the 4 × 4 2-D Butler matrix [14].

3.3.4 MS QWL

The output ports $j = 5$ to 8 of the Butler matrix are transformed to 50 Ω using 70.7 Ω QWLs to match them to 50 Ω antenna elements, as shown in Figure 3.6. The vias at the output ports, each have diameter a_f of 0.15 mm and serve to feed the elements. They are separated by distance $d = 1.86$ mm [13, 71]. Figure 3.7(a) shows a MS QWL with 50 and 100 Ω lines connected at its opposite ends. The simulated S-parameters for the structure is shown in Figure 3.5(b). The transmission coefficient is more than -0.5 dB indicating low loss and the reflection coefficients are less than -15 dB indicating a good match, across the whole band. The nature of the port field verifies that the structure is excited with quasi-TEM MS mode. The dimensions of the QWL is given in Table 3.2.



(a) (b)

Figure 3.7. MS quarter-wave transformer. (a) 3-D model with electric field vectors at 60 GHz at the ports. (b) Simulated S-parameters.

3.3.5 Simulation of Butler Matrix

The S-parameters of the Butler matrix are obtained by performing full-wave simulation in HFSS. The simulated reflection coefficient magnitude ($|S_{ii}|$) of the Butler matrix for all identical input ports i is -28 dB at 60 GHz and less than -10 dB across the band (56 to 67 GHz) indicating a broad impedance match, as shown in

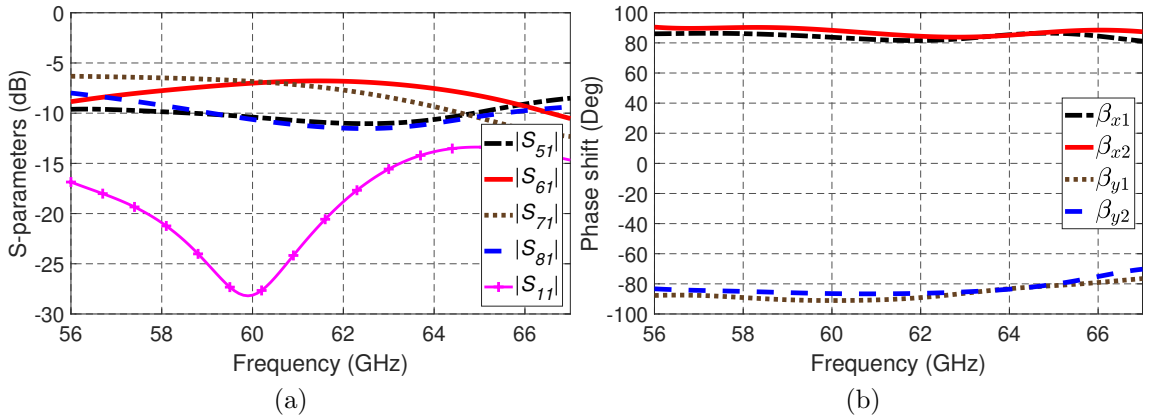
Figure 3.8(a). All the ports have identical reflection coefficients due to the symmetry.

A lossless 4 $\times$ 4 2-D Butler matrix divides the input power equally at its four output ports (i.e., -6 dB transmission coefficient). This decrease in transmission is not an actual loss since the divided power is recombined in the array main beam. In the presence of losses that are unavoidable in the MS implementation of the matrix, the input signal experiences different levels of path loss due to differences in the path lengths from the input to the outputs. Therefore, the transmission coefficients ($|S_{ji}|$) from input port $i = 1$, to output ports $j = 5$ to 8, shown in Figure 3.8(a), are not equal due to uneven losses. Using the -6 dB as the reference line, it can be seen that the actual loss (dielectric, conductor, and radiation losses) in the Butler matrix varies from 1 dB to 5 dB at the output ports at 60 GHz. The interelement phase shifts $(\beta_x)_i$ and $(\beta_y)_i$ for port i excitation can be derived from the phase difference between the transmission coefficients as follows:

$$(\beta_x)_i = \begin{cases} (\beta_{x1})_i = (\beta_{a_{2,1}})_i = (\beta_{87})_i = \angle S_{8i} - \angle S_{7i} \\ (\beta_{x2})_i = (\beta_{a_{4,3}})_i = (\beta_{56})_i = \angle S_{5i} - \angle S_{6i} \end{cases} \tag{3.2}$$

$$(\beta_y)_i = \begin{cases} (\beta_{y1})_i = (\beta_{a_{2,4}})_i = (\beta_{85})_i = \angle S_{8i} - \angle S_{5i} \\ (\beta_{y2})_i = (\beta_{a_{1,3}})_i = (\beta_{76})_i = \angle S_{7i} - \angle S_{6i} \end{cases} \tag{3.3}$$

For port $i = 1$ excitation, the interelement phase shifts $(\beta_{x1})_1$, $(\beta_{x2})_1$, $(\beta_{y1})_1$, and $(\beta_{y2})_1$ are plotted in Figure 3.8(b). At the design frequency of 60 GHz, it can be seen that $(\beta_{x1})_1 \approx +85°$, $(\beta_{x2})_1 \approx +90°$, $(\beta_{y1})_1 \approx -90°$, and $(\beta_{y2})_1 \approx -85°$. This matches the expected values in Table 3.1 within a small $\pm 5°$ margin. Moreover, the phase shifts are maintained over a wideband. The values in Table 3.1 are checked and verified for other port excitations but the results are not included here because of similarity with the plot shown and for conciseness.



(a) (b)

Figure 3.8. Magnitude and phase of the 4 × 4 2-D Butler matrix [14]: (a) Simulated S-parameters for port 1 excitation. (b) Simulated interelement phase shifts $(\beta_{x1})_1$, $(\beta_{x2})_1$, $(\beta_{y1})_1$, and $(\beta_{y2})_1$ at the matrix output when port 1 is excited.

Figure 3.9 shows the electric field distribution of the Butler matrix when port 1 is excited. The field distribution shown is under the hybrids and MS lines of the matrix. The power is split at each quadrature hybrid, and eventually reaches and gets distributed at the output ports. In Figure 3.10, fields in the vertical cut-plane containing a 90° hybrid and MS lines are shown, which indicate that the quasi-TEM MS modes are propagating on those structures. There is some coupling of the fields between the two arms of the hybrid.

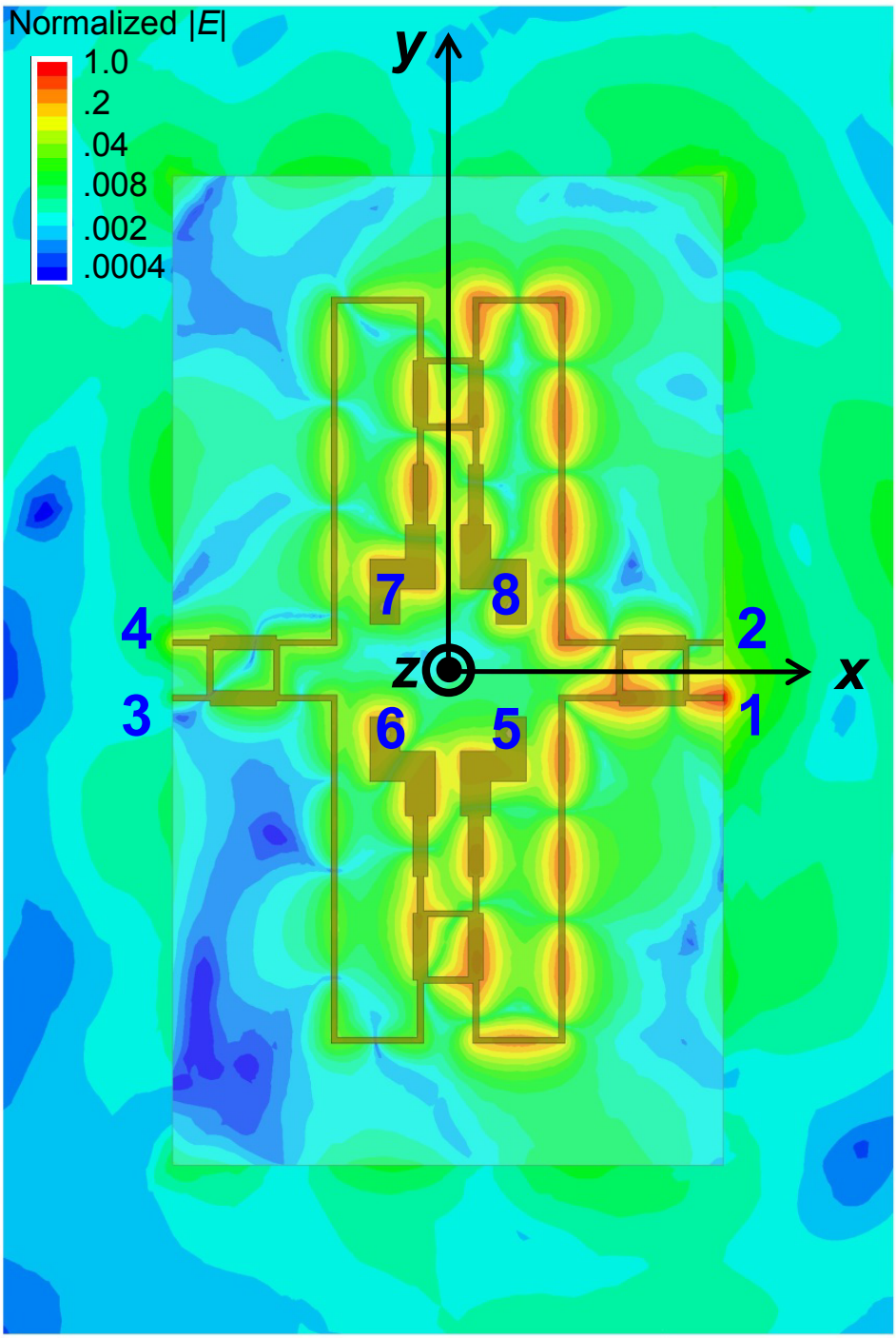


Figure 3.9. Surface plots of electric field distribution of the 2-D Butler matrix in log scale at 60 GHz. Fields shown are in the horizontal plane (at $z = h/2$) between the feed layer and ground plane.

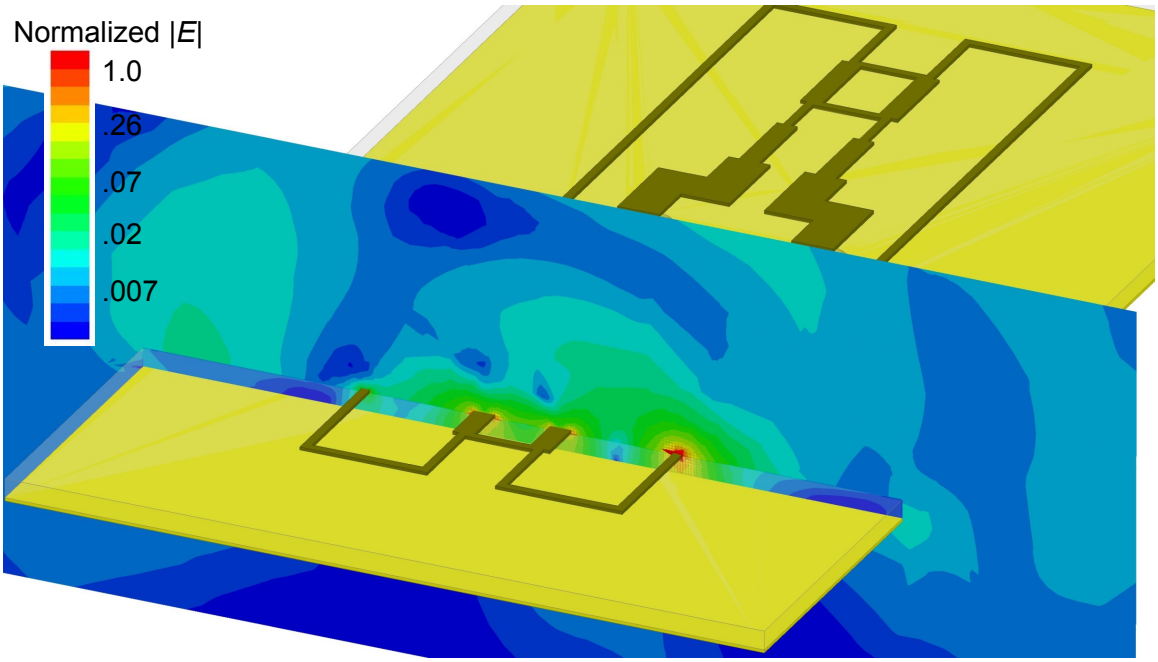
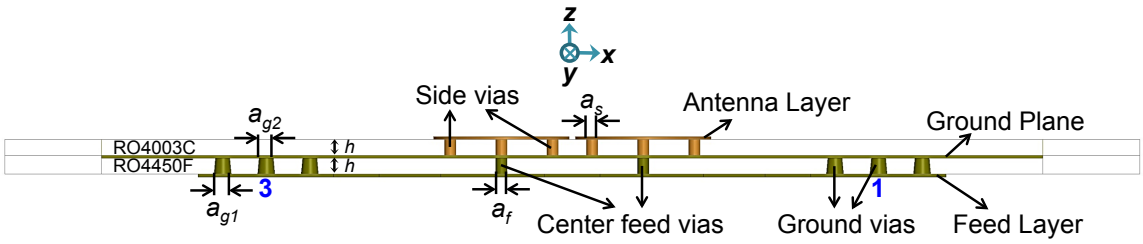


Figure 3.10. Surface plots of electric field distribution of the 2-D Butler matrix in log scale at 60 GHz. Fields shown are in the vertical plane crossing a hybrid and MS lines.

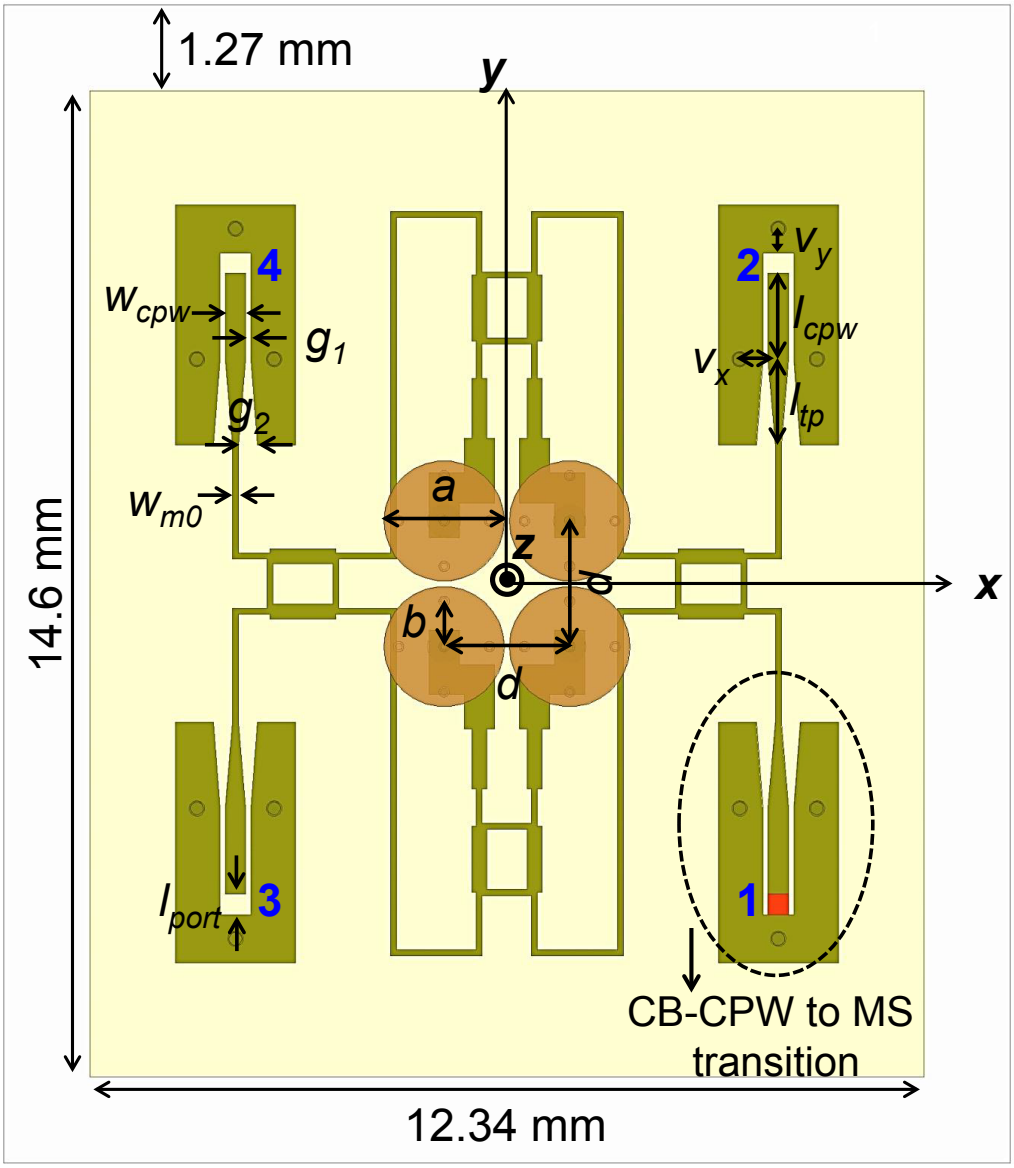
3.4 Packaging of Multilayer Antenna Module

Figure 3.11 shows the 3-D model of the circular patch planar array integrated with the Butler matrix, forming a multilayer antenna module. The top (antenna) layer of the 3-D model in Figure 3.11(a) and (b) shows the array. The Butler matrix (feed layer) of Figure 3.6 is stacked with the circular patch planar array of Figure 2.13 with their xy-planes aligned and the ground plane retained in between, to realize the multilayer antenna module, shown in Figure 3.11. The conductor-backed CPW (CB-CPW) to MS transitions are added at the inputs of the Butler matrix for measurement convenience, as is discussed in more detail in Section 3.4.1. The interelement separations, d_x and d_y are both fixed at $d = 1.86$ mm. The new ground plane size is 12.34 mm $\times$ 14.6 mm, and the substrate is further extended by 1.27 mm on all sides to meet the copper edge clearance requirement for fabrication. Specifically, the

extension keeps the copper traces from being too close to the board edge. This prevents lifting and damaging of the copper layers when cutting out the antenna module from the PCB panel after fabrication. The 3-D gain pattern of the module at 60 GHz when port 1 is excited, is shown in Figure 3.12.



(a)



(b)

Figure 3.11. 3-D model of the multilayer antenna module [14]. (a) Side view. (b) Top view.

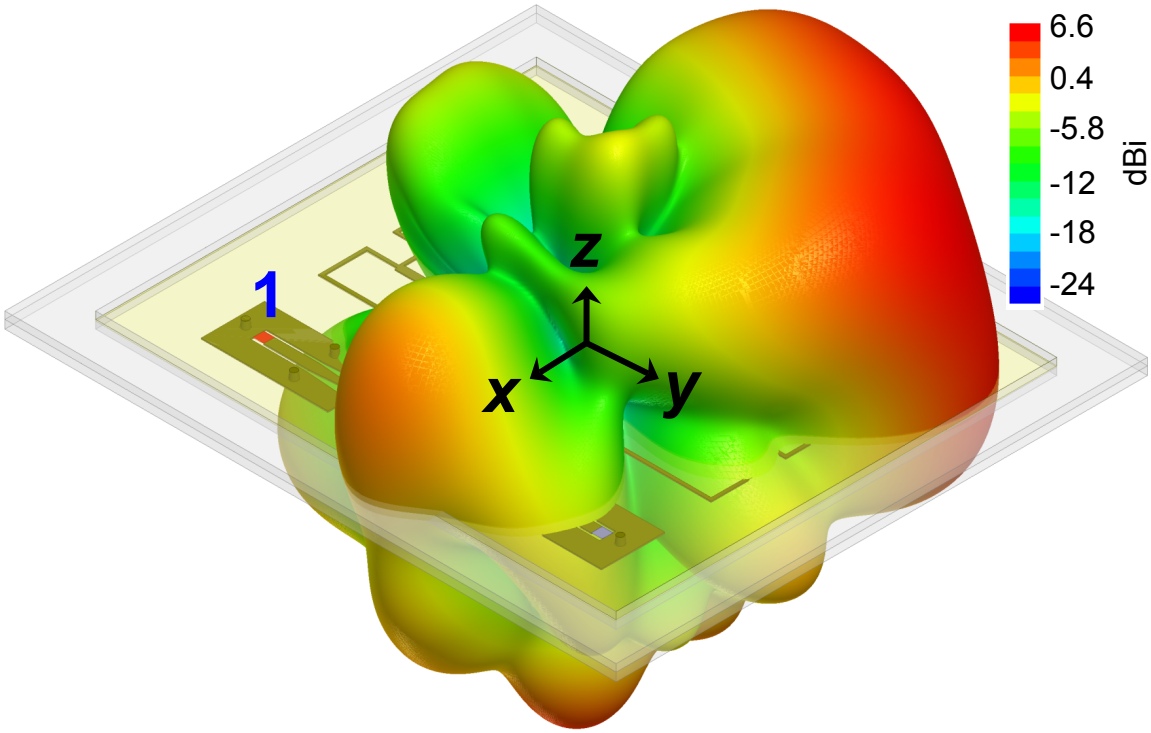


Figure 3.12. Simulated 3-D gain pattern (dB) of the module at 60 GHz for port 1 excitation [14].

The ground plane should shield and decouple the two layers from one another so that both the feed network and the antenna array work as designed with minimal performance changes after stacking and integration. The diameters of the center feed via a_f and four side vias a_s are 0.15 mm each and the side vias are located at radial distance $b = 0.67$ mm from the patch center [13]. As shown in Figure 3.11(a), each patch element on the antenna layer is center-fed from an output of the Butler matrix from the feed layer using the PTH via connection (of diameter a_f) through the ground plane. The antenna layer is printed on the Rogers RO4003C dielectric core. The RO4450F prepreg containing the Butler matrix (feed) layer is then stacked and bonded with the core. The ground plane is sandwiched between the feed and antenna layers. This integrates the Butler matrix of Figure 3.6 with the array. The realized multilayer antenna module, shown in Figure 3.11, is suitable for an AiP

implementation with the CMOS chips [17, 28, 32, 34]. The prepreg and the core each have thickness $h = 0.2$ mm with 35 μm copper finish. The AiP solution offers much higher radiation efficiency and SNR over an AoC implementation [27]. The antenna module can be surface mounted on the PCB board using solder balls to connect the inputs of the Butler matrix on the feed layer to the transceiver circuits on the CMOS chip. The solid ground plane not only helps to minimize interference by blocking antenna radiation into the feed layer and CMOS circuits underneath, but it also decouples the antenna and feed layer. This greatly simplifies the design process since the antenna array and Butler matrix can be designed independently of one another and stacked together afterwards without significant performance degradation. Figure 3.13 shows the simulated $|S_{11}|$ of the antenna module. A simulated impedance BW of more than 11 GHz is seen. An impedance BW of 8.25 GHz is measured. The measured $|S_{11}|$ is presented later in Section 5.2.3.

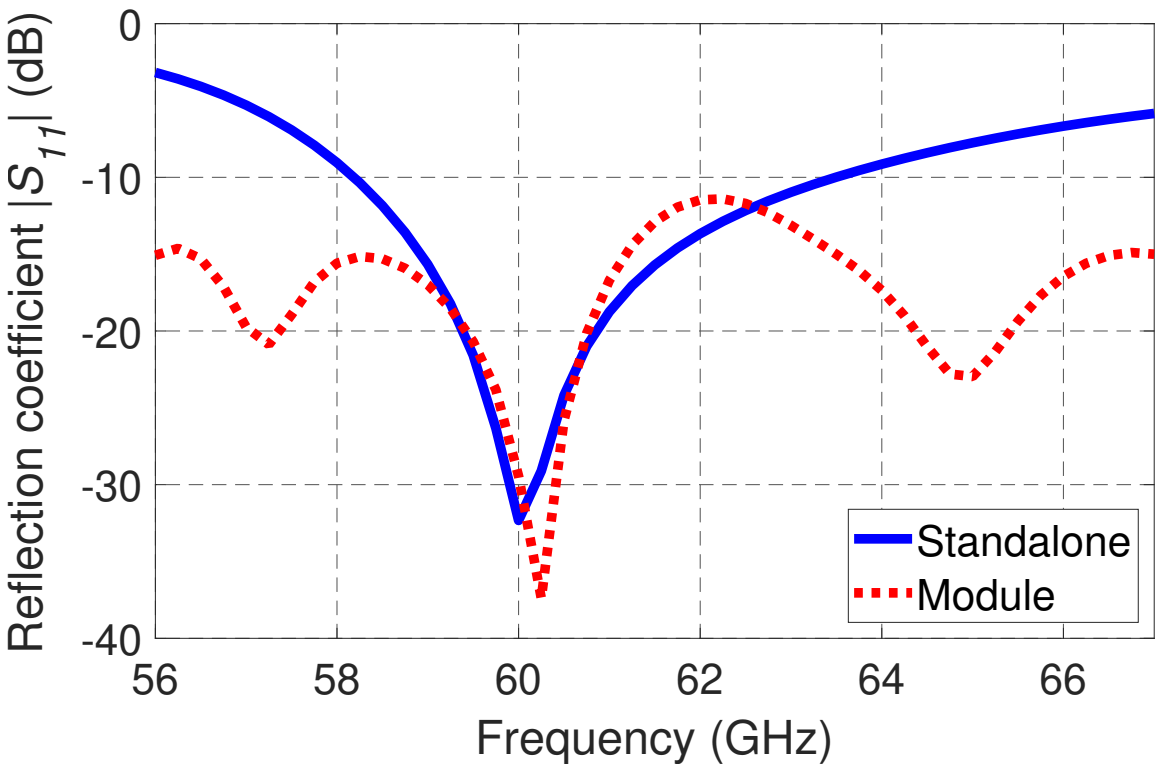


Figure 3.13. Simulated reflection coefficient magnitude (dB) of the antenna module and the standalone array (at one of the patch elements).

3.4.1 CB-CPW to MS Transitions

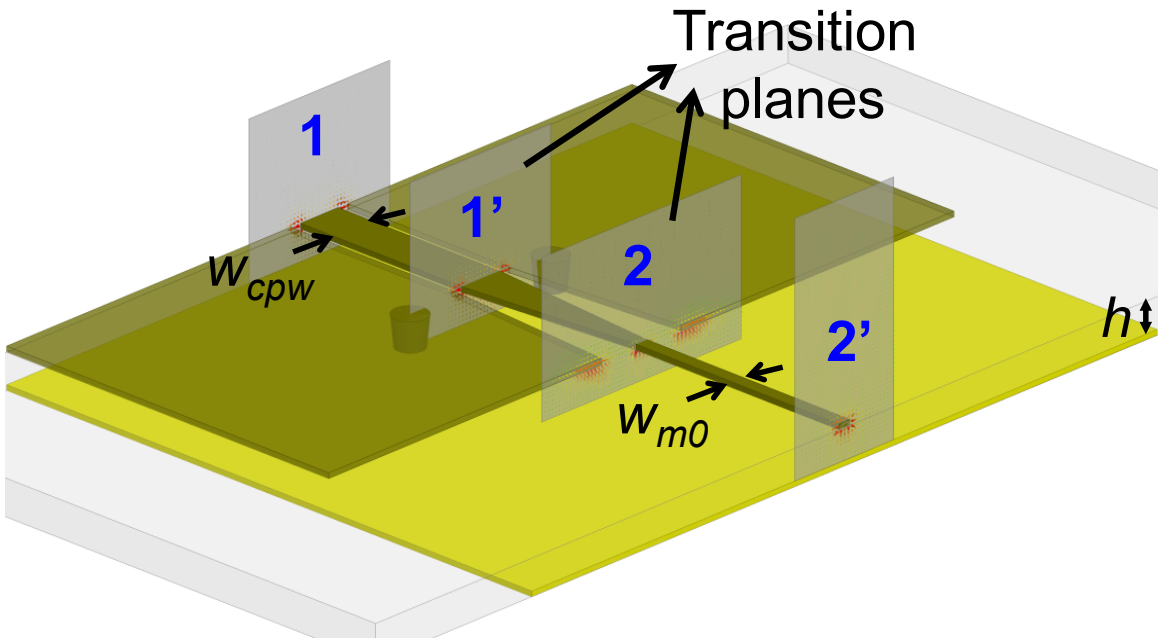
To transform the input port impedance from 100 to 50 Ω, CB-CPW to MS transitions are augmented at the input of the Butler matrix, as shown in Figure 3.11(b). The CB-CPW pads provide a compatible, stable and convenient interface for the ground-signal-ground (GSG) probes of a network analyzer when making measurements [41, 70]. In this dissertation, the CB-CPW feed lines are probed using 250 μm pitch GSG probes. In order to achieve a smooth and broadband transition, the 100 Ω MS lines are connected to the 50 Ω CB-CPW lines by linearly tapering the width of the interconnecting lines from w_{m0} to w_{cpw} and the gap from g_2 to g_1, as shown in Figure 3.11(b). The gap g_2 is adjusted to improve the reflection coefficient magnitude (at 60 GHz) and the impedance BW of the transitions. The linear tapering of the

width w and gap g along the length l of the taper are implemented in HFSS using the following equations:

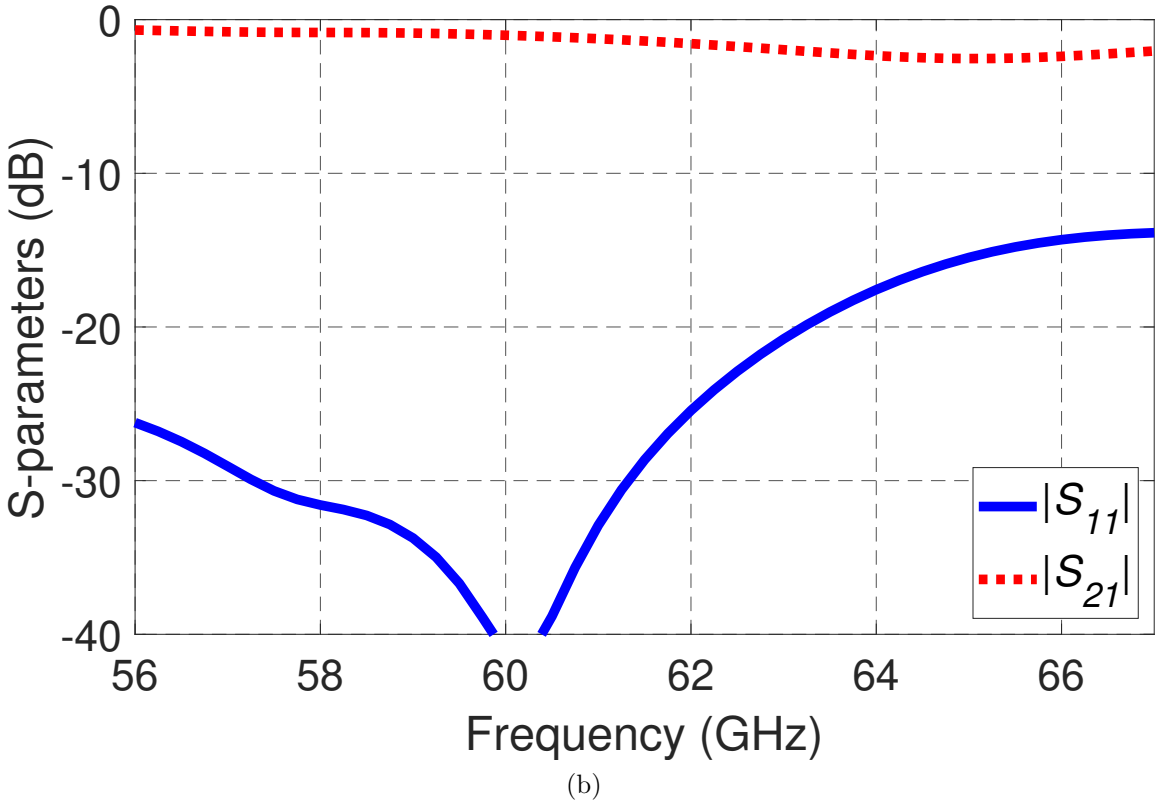
$$w = \frac{w_{m0} - w_{cpw}}{l_{tp}} l + w_{cpw} \qquad 0 \leq l \leq l_{tp} \tag{3.4}$$

$$g = \frac{g_2 - g_1}{l_{tp}} l + g_1 \qquad 0 \leq l \leq l_{tp} \tag{3.5}$$

See Appendix B for derivation. The line impedances are all verified from full-wave simulation. The side and back traces of the CB-CPW lines must be grounded by connecting them to the ground plane layer. This is done by using three ground vias (laser drilled) for each CB-CPW line, as shown in Figure 3.11(a). Figure 3.14(a) shows the 3-D model of an isolated CB-CPW to MS transition created in HFSS and is identical to the ones shown in Figure 3.11(a) and (b). Within the frequency range considered, the simulated transmission coefficient of the isolated transition [from port 1 to 2 in Figure 3.14(a)] is no less than -1 dB with a good impedance match, as shown in Figure 3.14(b). The gradual widening of the gap from g_1 to g_2 provides a smooth transition between the field lines of the quasi-TEM CPW (two peaks on the sides of the center trace) and quasi-TEM MS (one peak around the center trace) modes, as shown in Figure 3.15. This reduces the field distribution mismatch between the two transmission line types. The wider gap g_2 has caused the quasi-TEM CPW field at the transition plane/port 2 to look more like a quasi-TEM MS field (around the center trace) at plane 2'.



(a)



(b)

Figure 3.14. CB-CPW to MS transition. (a) 3-D model with electric field vector plot at 60 GHz at the ports and transition planes. (b) Simulated S-parameters [14].

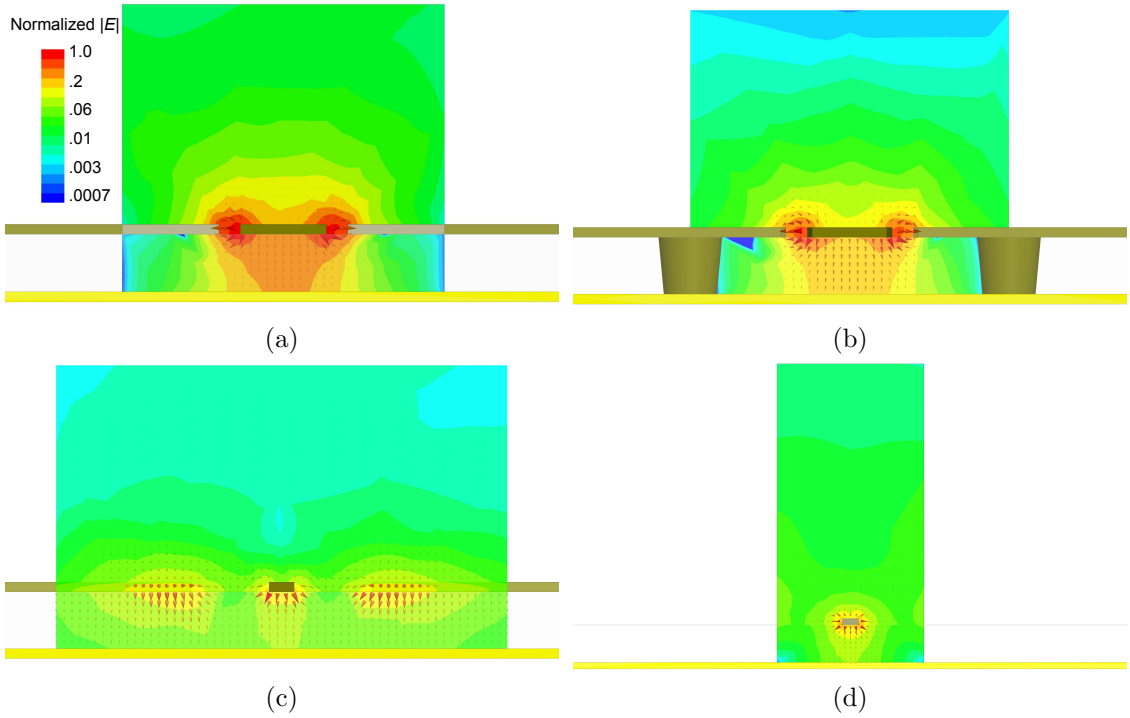


Figure 3.15. Electric field distribution of the CB-CPW to MS transition at 60 GHz: (a) Quasi-TEM CPW at port 1. (b) Quasi-TEM CPW at the transition plane 1'. (c) Quasi-TEM CPW at the transition plane/port 2. (d) Quasi-TEM MS at plane 2'.

The key dimensions of the CB-CPW to MS transitions are labeled in Figure 3.11(b) and summarized in Table 3.3.

Table 3.3. Dimensions associated with the CB-CPW to MS transition

Definition	**Dimension**	**Value (mm)**
Width of 50 Ω CB-CPW line	w_{cpw}	0.3
Length of 50 Ω CB-CPW line	l_{cpw}	1.27
Length of CB-CPW port	l_{port}	0.3
Length of the taper	l_{tp}	1.27
Diameter of ground vias at the feed layer	a_{g1}	0.23
Diameter of ground vias at the ground plane	a_{g2}	0.19
CPW trace/side ground gap (CPW end)	g_1	0.08
CPW trace/side ground gap (MS end)	g_2	0.28
Location of ground vias [see Figure 3.11(b)]	(v_x, v_y)	(0.57, 0.36)

A linear taper is just a special case of the quadratic taper. As derived in Appendix B, the quadratic tapering of width w and gap g, once the taper factors $d_w > 0$ and $d_g > 0$ are specified, can be attained as

$$w = \frac{2[w_{m0}(1-2d_w)+w_{cpw}]}{l_{tp}^2}l^2 + \frac{w_{m0}(4d_w-1)-3w_{cpw}}{l_{tp}}l + w_{cpw} \qquad 0 \le l \le l_{tp} \quad (3.6)$$

$$g = \frac{2[g_2(1-2d_g)+g_1]}{l_{tp}^2}l^2 + \frac{g_2(4d_g-1)-3g_1}{l_{tp}}l + g_1 \qquad 0 \le l \le l_{tp} \quad (3.7)$$

The impedance profiles of the linear, quadratic (with $d_w = 1.6$ and $d_g = 0.2$), and Klopfenstein (optimal) tapers [24] are shown in Figure 3.16. The linear and quadratic profiles are calculated using the analytical expression for the characteristic impedance of the CB-CPW structure (given its geometry) that can be found in [81] and also given in Appendix C. The Klopfenstein profile is calculated using the equations given in [24] for $|S_{11}| \le -34$ dB. The quadratic taper can be designed to closely approximate the Klopfenstein taper. But it can be difficult to realize, especially since it has a narrow taper gap at the midpoint, i.e., $g = d_g g_2 = 0.056$ mm at $l = l_{tp}/2$, which is hard to achieve with PCB fabrication. The linear taper has an impedance profile that is not too far from the Klopfenstein and it has wider taper gaps, which are easily realizable with the PCB techniques. Therefore, it is chosen for the impedance matching purpose.

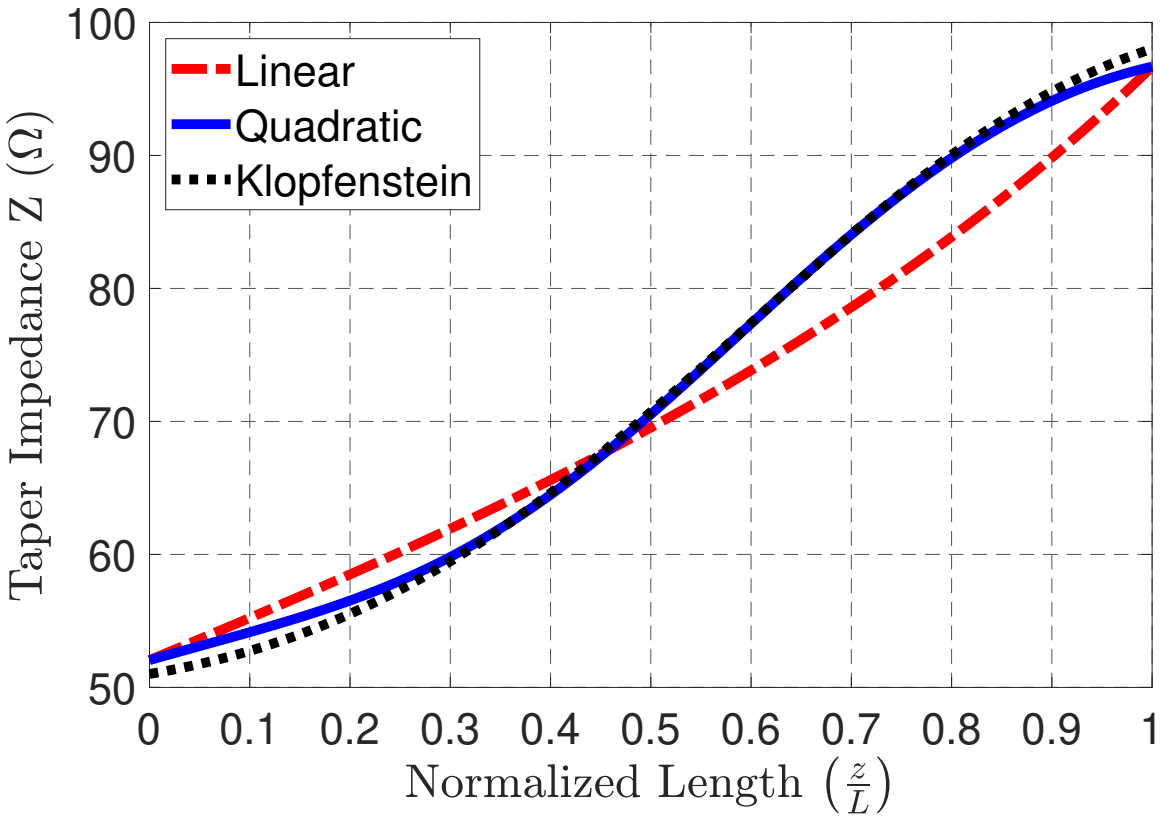


Figure 3.16. Variations of impedance for the linear, quadratic, and Klopfenstein tapers. The Klopfenstein taper shown is specified to have $|S_{11}| \leq -34$ dB in the passband.

Figure 3.17 shows the time-domain reflectometry (TDR) impedance of the CB-CPW to MS transition with linear taper, which is generated in HFSS with the excitation at the CB-CPW end. A gradual change in impedance from 50 to 100 Ω is seen, as the signal travels from the CB-CPW end, through the tapered portion of the transition and to the MS end.

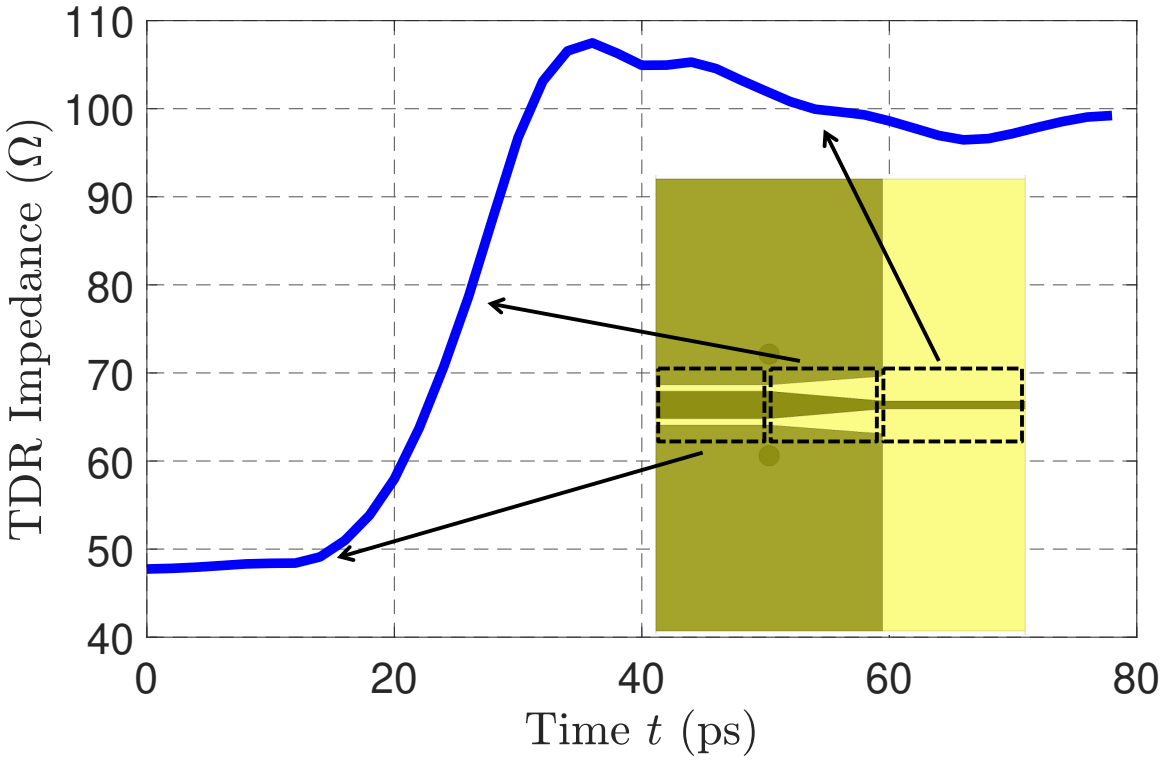


Figure 3.17. TDR impedance of the CB-CPW to MS transition.

The TDR impedance is calculated as the ratio of instantaneous time-domain voltage $v(t)$ to the current $i(t)$. These time-domain quantities are obtained by taking the inverse fast Fourier transform (IFFT) of their respective frequency-domain counterparts $V(f)$ and $I(f)$ in HFSS. The frequency-domain data is obtained by performing a full-wave simulation with an interpolating sweep from DC to f_{max} in Δf steps where f_{max} depends on the time step Δt as

$$f_{max} = \frac{1}{2\Delta t} \tag{3.8}$$

and the time step Δt is set to be a fraction of the rise time of the step signal τ as

$$\Delta t = \frac{\tau}{N_\tau} \tag{3.9}$$

where N_τ is the number of time steps per signal rise time and the maximum plot time T is given by

$$T = N\Delta t \tag{3.10}$$

where N is the number of time samples. A signal rise time of $\tau = 10$ ps with $\Delta t = 2$ ps [corresponding to $f_{max} = 250$ GHz from (3.8)] is enough for the signal to have sufficient time and spatial resolution to obtain a smooth TDR response. A maximum plot time of $T = 80$ ps ($N = 40$) is used, which is long enough for the signal to travel the total length of the structure several times and thus generate a complete TDR response. The frequency step Δf for the simulation can be calculated as

$$\Delta f = \frac{f_{max}}{10N} \tag{3.11}$$

$\Delta f = 0.625$ GHz is obtained from (3.11) and is used in the simulation. A Hanning window of 100% width is applied on the time-domain signal to reduce the high-frequency artifacts due to the inherent signal truncation and generate a smoother TDR response. Nonetheless, there are oscillations after 60 ps in the TDR plot. This is due to the signal undergoing multiple reflections between discontinuities before reaching back at the CB-CPW end.

3.4.2 Switching of the Antenna Module Main Beam

The CB-CPW inputs are individually excited to switch the main beam of the module. Each port excitation attains a combination of interelement phase shifts given in Table 3.1 and produces a main beam in one of the four diagonal directions. The beam switching can be seen in the horizontal gain patterns ($\theta = 90°$) shown in Figure 3.18. The antenna module has an endfire main beam with a peak gain of 5.3 dBi at 60 GHz along the diagonal directions (ϕ_0). This gain is with the Butler matrix and CPW transitions included. The maximum SLL is 4.64 dB.

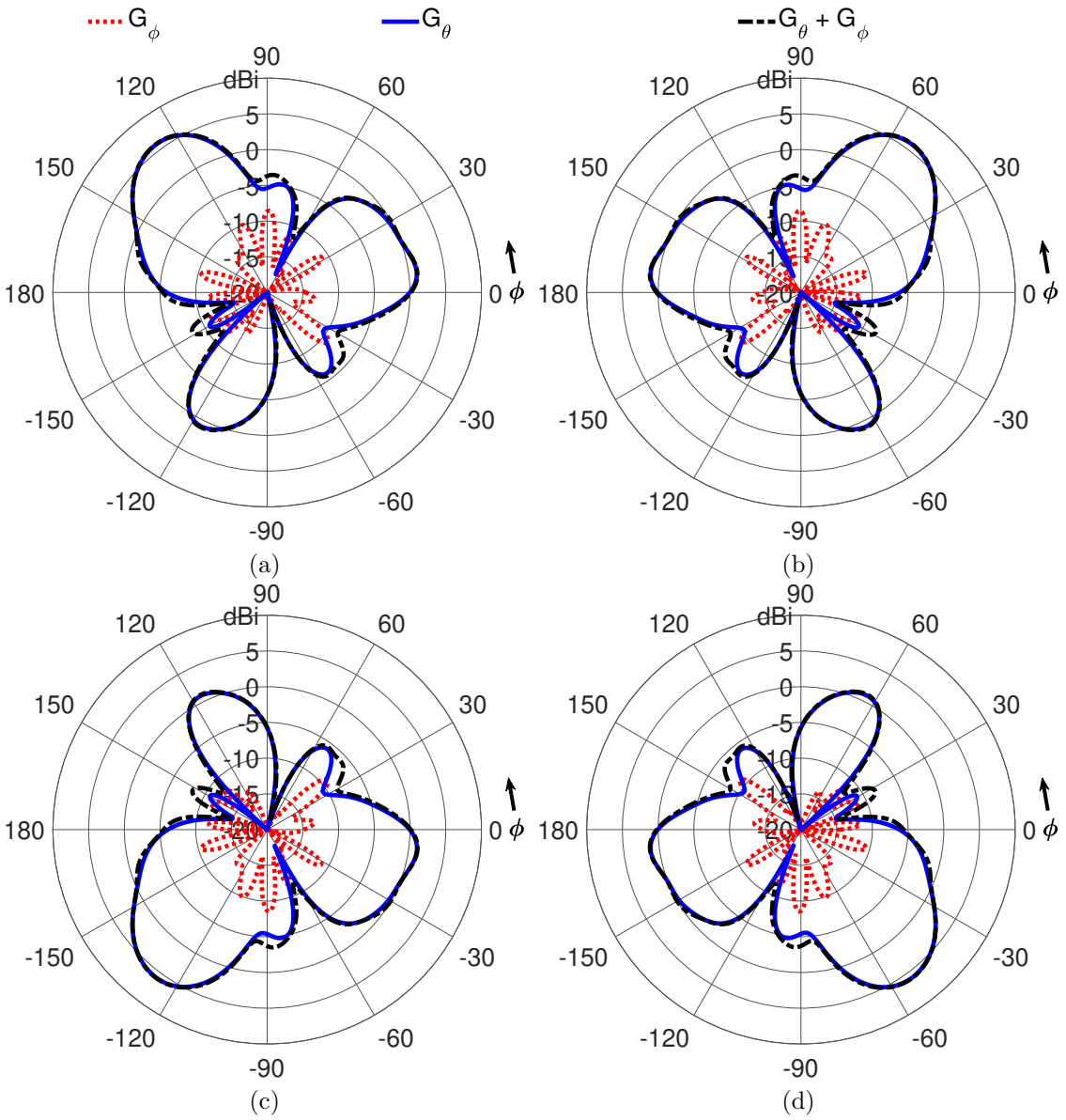


Figure 3.18. Simulated gain patterns (dBi) of the antenna module at 60 GHz in the horizontal plane ($\theta = 90°$) [14]: (a) Port 1 ($\phi_0 = +135°$). (b) Port 3 ($\phi_0 = +45°$). (c) Port 2 ($\phi_0 = -135°$). (d) Port 4 ($\phi_0 = -45°$).

In order to isolate the effect of the feed layer, the antenna array without the feed network (standalone) but having the same ground plane size as the module is simulated. The 3-D model and horizontal gain patterns are shown in Figures 3.19 and 3.20, respectively. Figure 3.13 compares the simulated $|S_{11}|$ of the standalone

array with that of the module. The module has higher impedance BW because of additional losses (decreased Q) in the feed layer. The gain BW, however, will be reduced, as is discussed in more detail in Section 3.6.

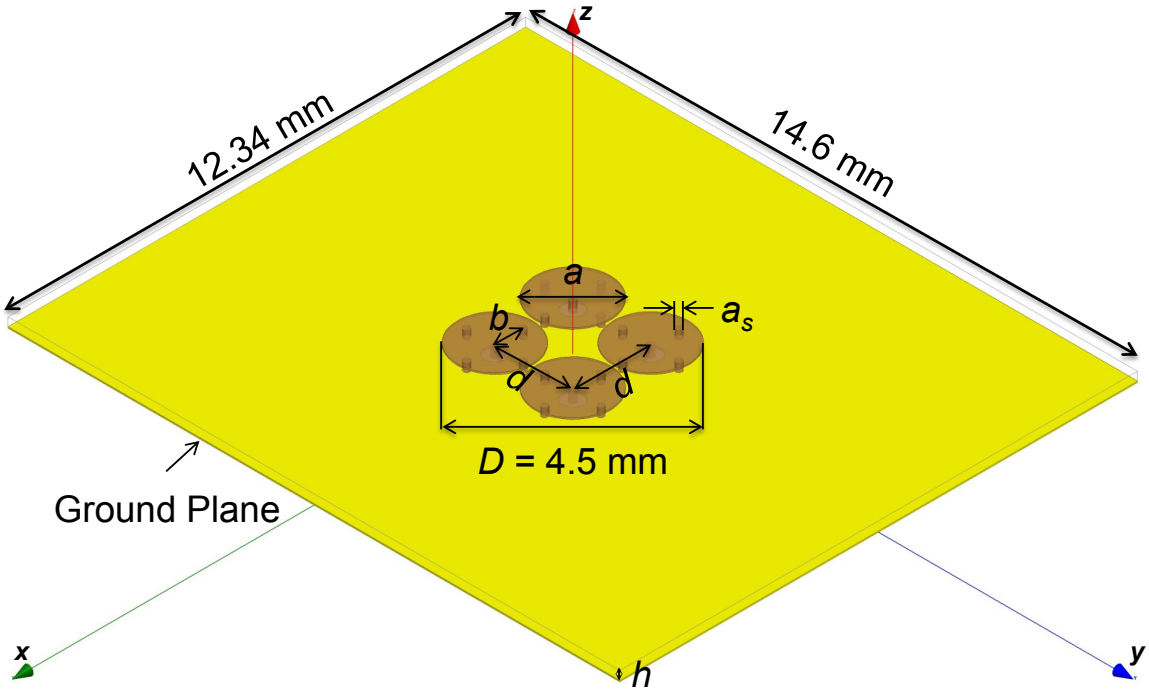


Figure 3.19. 3-D model of the standalone 2 × 2 circular patch planar array having the ground plane size same as that of the module.

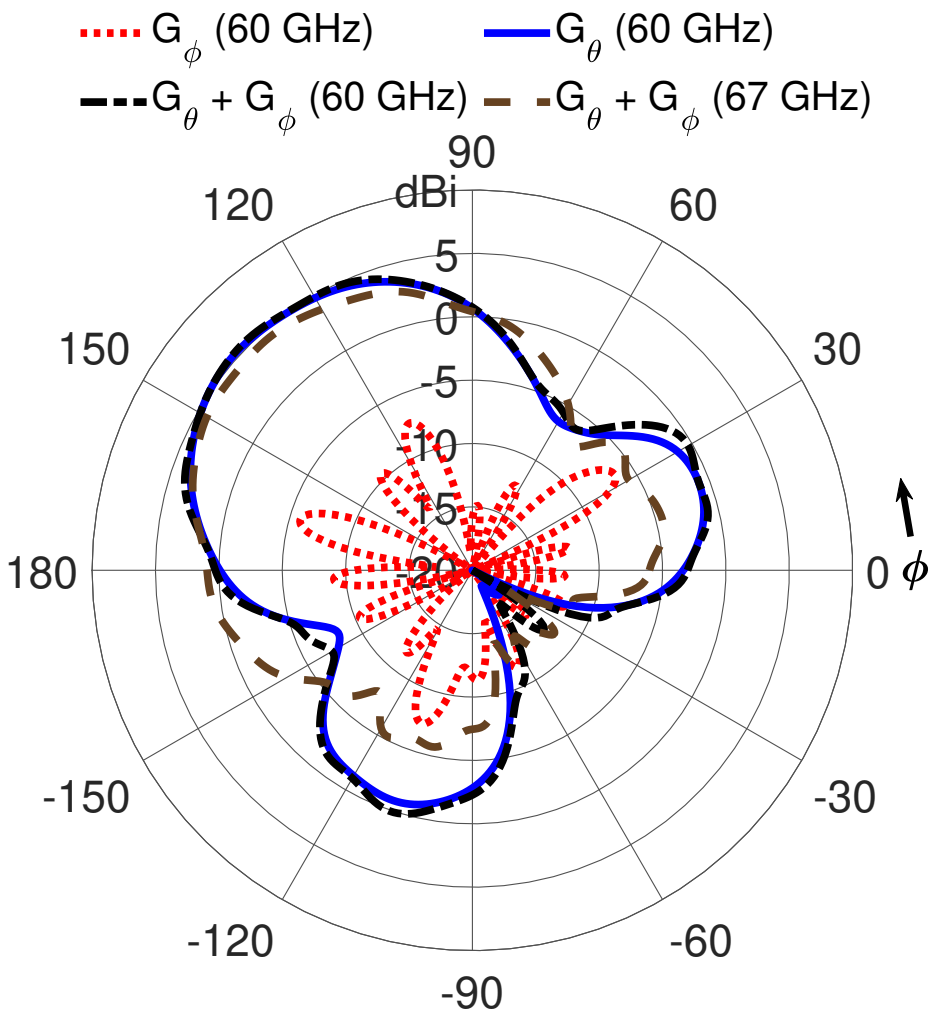


Figure 3.20. Simulated gain patterns (dB) of the standalone array at 60 and 67 GHz in the horizontal plane ($\theta = 90°$). The phase shifts obtained at the matrix output are used for the 67 GHz pattern. The 67 GHz pattern shows beam broadening relative to the 60 GHz pattern.

Figure 3.21 shows the electric field under the patches of the standalone array and it is interesting to see how each element of the array contributes to the main beam along the diagonal $\phi_0 = 135°$. The field distribution under each patch has some similarity with that of the isolated patch, shown in Figure 2.8(b), but is not as azimuthally symmetric due to mutual coupling. The pair of two patches on either side of the diagonal have similar field levels because they are in-phase. The pair of two patches

on the diagonal have different field levels because they are 180° out-of-phase. The two pairs are 90° out-of-phase. These can be proved using Table 3.1 for port 1 excitation.

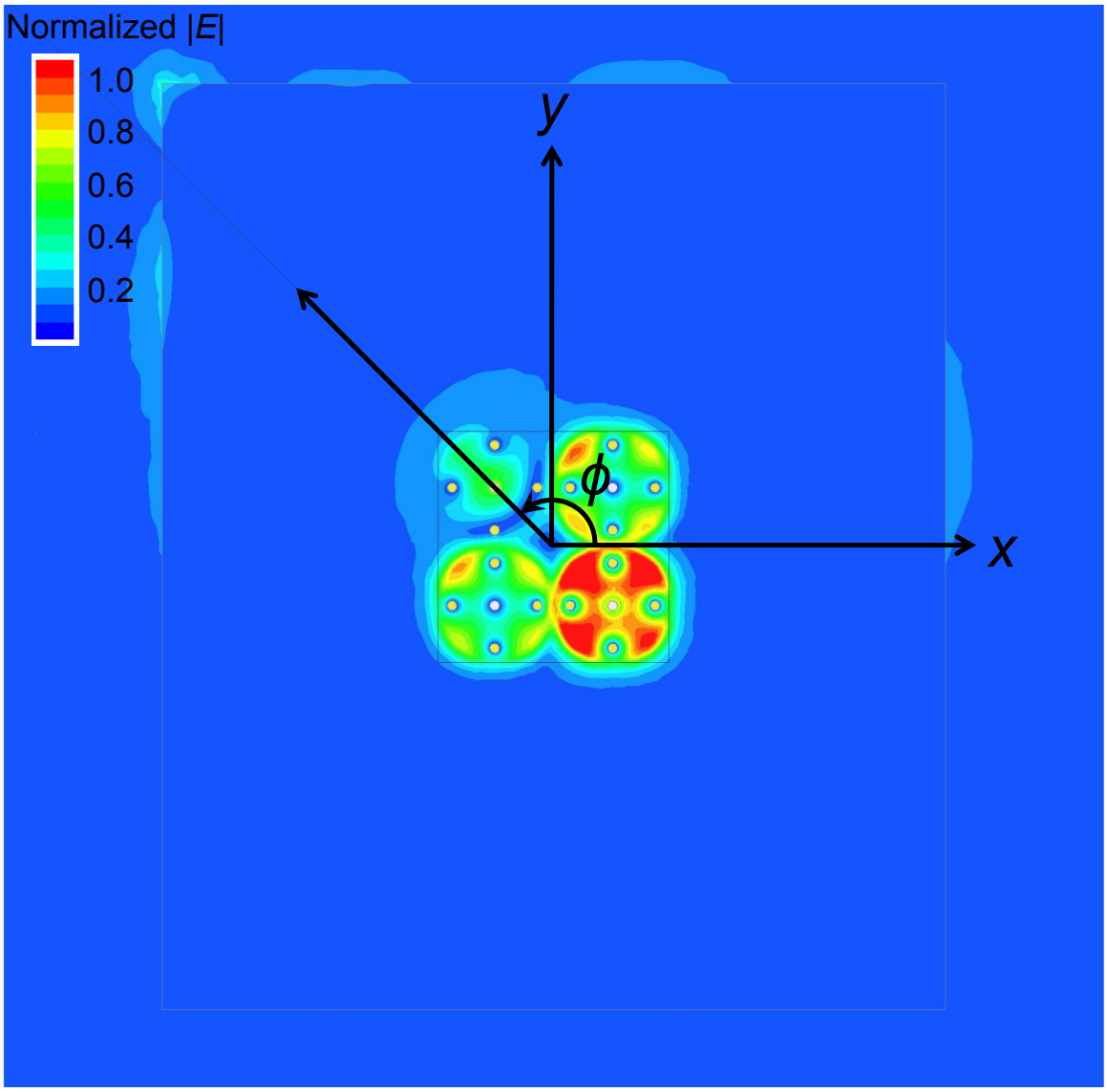


Figure 3.21. Electric field distribution of the standalone array in the $z = h/2$ horizontal plane (i.e., between the antenna layer and ground plane).

Comparing Figures 3.18(a) and 3.20, one can see that the presence of the feed layer has reduced the peak gain slightly and increased the SLL. Also, the radiation from the feed layer has caused the pattern in Figure 3.18(a) to be more directive and

asymmetric than the pattern in Figure 3.20. The antenna module, like the standalone array, radiates mostly in the G_θ polarization (around 19 dB higher than the G_ϕ polarization) along the diagonal directions. The highest G_ϕ level of the antenna module has reduced to 14 dB below the peak gain (compared to just 11 dB for the standalone array). The feed layer losses and radiation have decreased the overall G_θ and G_ϕ levels in the horizontal plane. This can be better understood from the gain patterns of the standalone array and the module in the vertical plane containing the main beam (i.e., $\phi = 135°$), as shown in Figure 3.22. The module has higher back and side lobes (i.e., below the ground plane) due to the radiation from the MS lines of the feed layer. The radiation from the feed layer has increased the overall G_θ and G_ϕ levels of the module below the ground plane and directed some of the radiation away from the horizontal plane. As a result, the horizontal pattern shown in Figure 3.18(a) has decreased G_θ and G_ϕ levels compared to Figure 3.20.

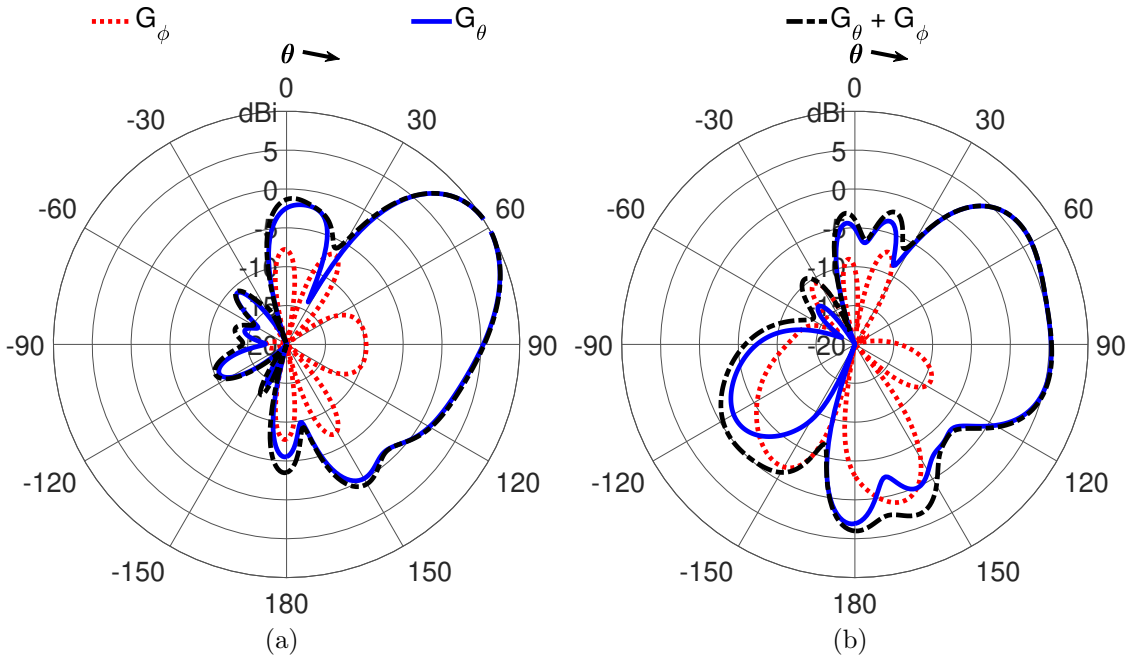


Figure 3.22. Simulated gain patterns (dBi) at 60 GHz in the vertical plane ($\phi = 135°$). (a) Standalone array. (b) Antenna module.

The overall gain (G_{mod}) of the module along the main beam direction can be written as [21]

$$G_{mod}(\theta, \phi) = e_{mod} D_{mod}(\theta, \phi) \tag{3.12}$$

where e_{mod} and D_{mod} are the radiation efficiency and directivity, respectively, of the array combined with the feed network.

The module achieved a simulated $e_{mod} = 76\%$ at 60 GHz. Note that e_{mod} is lower than $e_r = 96\%$ of the standalone array because the module includes the feed layer whose losses are taken into account when determining the overall efficiency. Both the efficiencies stay fairly constant over the frequency range, as shown in Figure 3.23.

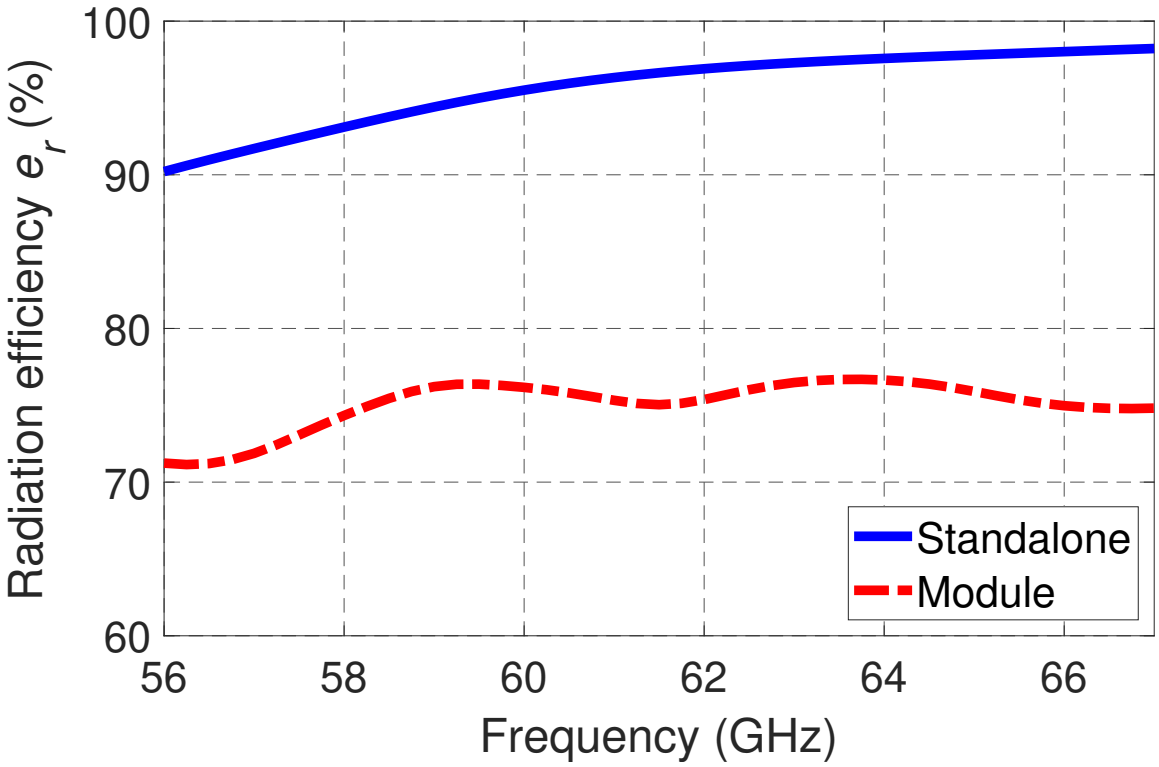


Figure 3.23. Radiation efficiency (simulated) variation of the standalone array and the module.

To increase the directivity of the array, the interelement separation d can be increased or more elements can be used with relatively slight increase in the array

footprint. However, a larger feed network will be required, and the feed losses will increase as well. To ensure an overall increase in G_{mod}, the factor by which D_{mod} increases must be greater than the factor by which e_{mod} decreases. Having more elements will also increase the number of switchable beams. The performance of the standalone array and the module is summarized in Table 3.4.

Table 3.4. Performance metrics (simulated) of the circular patch planar array without and with the feed network

Antenna Metric	**Standalone**	**Module**
Peak horizontal gain	5.5 dBi	5.3 dBi
$\|S_{11}\|$ BW	5.25 GHz	>11 GHz
Realized gain BW	> 11 GHz	6.75 GHz
Radiation efficiencies e_r and e_{mod}	96%	76%
Peak cross pol. (G_ϕ) (horizontal)	-5.5 dBi	-8.7 dBi
Vertical plane HPBW	38°	75°
Horizontal plane HPBW	73°	35°
Vertical plane FNBW	110°	106°
Horizontal plane FNBW	157°	132°
Vertical plane max. SLL	9.35 dB	2.31 dB
Horizontal plane max. SLL	5.36 dB	4.64 dB

3.5 Field Visualization of Waves

The presence of a common ground plane and substrate causes significant surface wave coupling between the circular patch antenna arrays. The relative contribution of space wave (radiation) and surface wave to the total link power is studied in [82,83] for various antenna types. The surface waves are the TM^z and TE^z guided modes of the grounded dielectric substrate [84]. For the substrate (core) parameters $\epsilon_r = 3.55$ and $h = 0.2$ mm, only the TM_0^z can be excited at 60 GHz since all the higher order TM^z and TE^z modes are cut off. The cutoff frequency f_c of a grounded dielectric substrate [84] can be found using

$$(f_c)_m = \frac{m}{4h\sqrt{\mu_0\epsilon_0}\sqrt{\mu_r\epsilon_r - 1}} \qquad \begin{cases} m = 0, 2, 4, ..., \text{TM}_m^z \\ m = 1, 3, 5, ..., \text{TE}_m^z \end{cases} \tag{3.13}$$

The lowest order (dominant) mode is the TM_0^z, which has a zero cutoff frequency from (3.13). The fields under the patch metal will always excite this mode even on thin substrates with low dielectric constant, as illustrated in Figure 3.24.

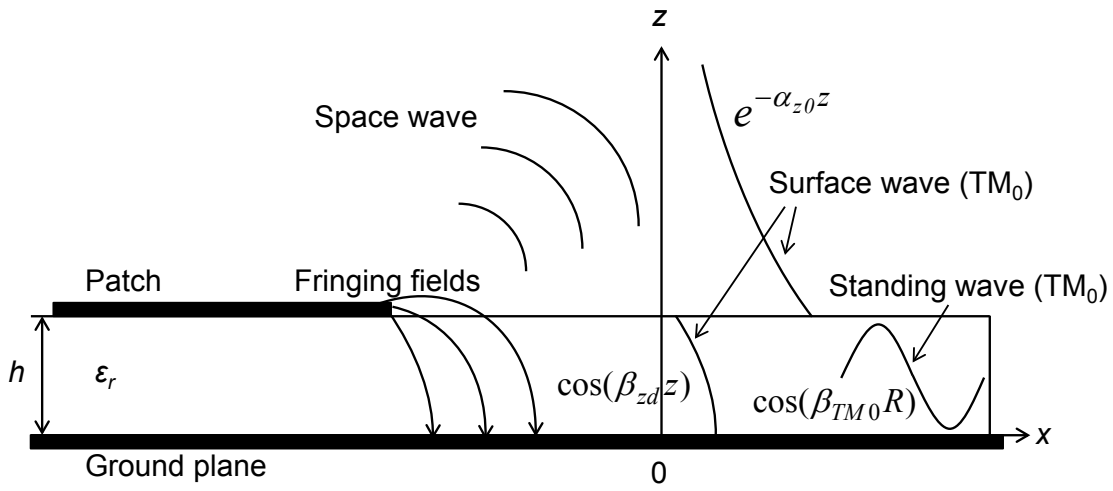


Figure 3.24. Field distribution of the TM_0^z mode in a grounded dielectric substrate along with radiation from a MS antenna [83].

The propagation wavenumber β_{TM_0} for the TM_0^z mode can be found by numerically solving the characteristic equation of the grounded dielectric substrate, which is given by [84]

$$\epsilon_r \alpha_{z0} = \beta_{zd} \tan(\beta_{zd} h) \tag{3.14}$$

where α_{z0} and β_{zd} are the air attenuation coefficient and dielectric wavenumber, respectively. They are related to β_{TM_0} by the separation equations as follows:

$$\alpha_{z0}^2 = \beta_{TM_0}^2 - k_0^2 \tag{3.15}$$

$$\beta_{zd}^2 = \epsilon_r k_0^2 - \beta_{TM_0}^2 \tag{3.16}$$

The k_{TM_0} obtained from (2.55) is the same as β_{TM_0} i.e., $k_{TM_0} = \beta_{TM_0}$, albeit using different techniques. Table 3.5 lists the solved values of the wavenumbers and attenuation coefficients of the TM_0^z mode at 60 GHz.

Table 3.5. Wavenumbers and attenuation coefficient of the TM_0^z mode

Parameter	**Value**
β_{TM_0}	$1.02k_0$
β_{zd}	$1.59k_0$
α_{z0}	$0.19k_0$

The next higher order mode TE_1^z has a cutoff frequency $(f_c)_1 = 235$ GHz, as calculated using (3.13). It cannot propagate below that frequency. The z-component of the electric field of the TM_0^z surface wave in the air and dielectric respectively are as follows [84]:

$$E_z^0 = -j\frac{\beta_{TM_0}^2}{\omega\mu_0\epsilon_0}A^d\cos(\beta_{zd}h)e^{-\alpha_{z0}(z-h)}e^{-j\beta_{TM_0}x} \quad h \leq z < \infty \tag{3.17}$$

$$E_z^d = -j\frac{\beta_{TM_0}^2}{\omega\mu_0\epsilon_0\epsilon_r}A^d\cos(\beta_{zd}z)e^{-j\beta_{TM_0}x} \quad 0 \leq z \leq h \tag{3.18}$$

where A^d is a constant that depends on the excitation and can also be assigned a value to normalize the fields so that $|E_z^d| = 1$ at the peak point $z = h$.

At the air-dielectric interface $z = h$, the normal, i.e., z-components of the electric flux densities in air D_z^0 and dielectric D_z^d have to be equal, which is a boundary condition [84]. This means there is a discontinuity between the corresponding electric field components E_z^0 and E_z^d at the interface, as illustrated in Figure 3.24. Mathematically,

$$D_z^0 = D_z^d\big|_{z=h} \tag{3.19}$$

$$E_z^0 = \epsilon_r E_z^d\big|_{z=h} \tag{3.20}$$

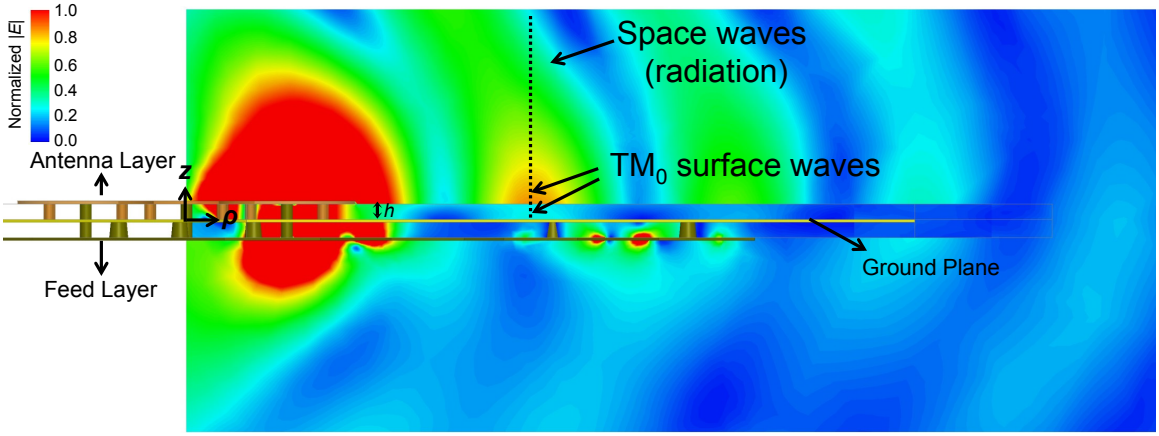
The TM_0^z mode when it reaches the substrate edge is reflected back (due to the substrate's finite extent) creating a standing wave pattern in the substrate. The standing waves can cause oscillations in the power coupling between two patch arrays on a common grounded substrate [83]. In air, this mode is diffracted at the edges and radiated away. Furthermore, there is a direct space wave (radiation) in air due to fringing fields from the patch metal to the ground plane, as illustrated in Figure 3.24.

The electric field of the dominant TM^z_{000} mode of the center-fed circular patch with side vias can easily couple to the TM^z_0 mode of the substrate, and thus, excite the surface waves. The electric field of the TM^z_{000} mode of the center-fed circular patch can be expressed as follows:

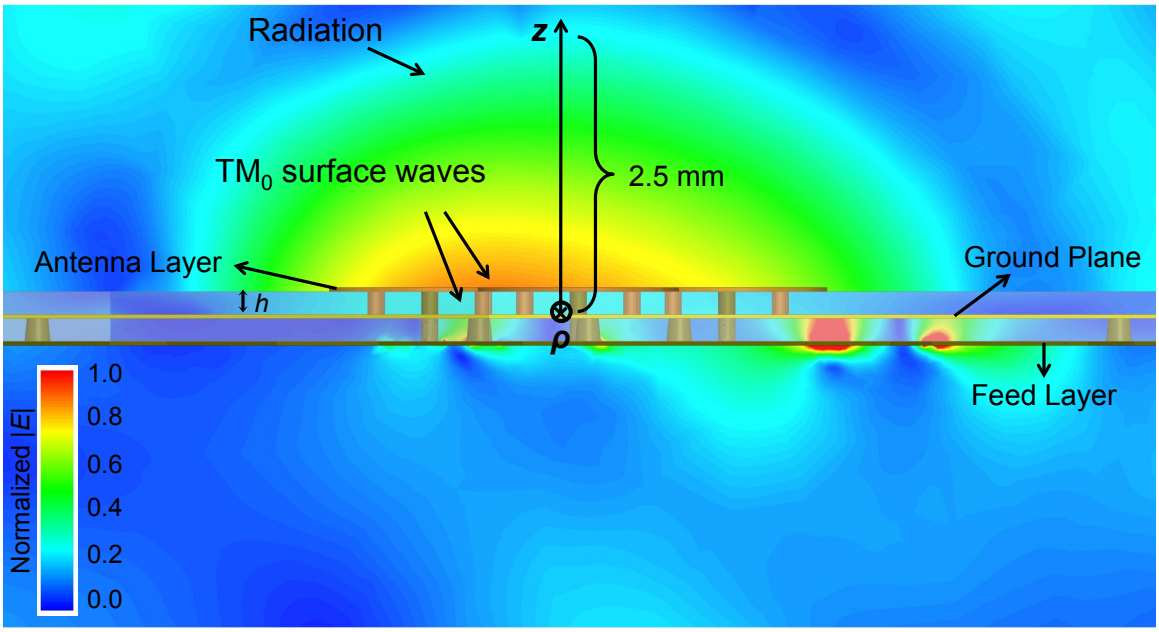
$$E_z^{ant} = BH_0^{(2)}(\beta_{TM_0}\rho) \overset{\rho\gg\lambda}{\approx} B\sqrt{\frac{2j}{\pi\beta_{TM_0}\rho}}e^{-j\beta_{TM_0}\rho} \tag{3.21}$$

where B is a constant that depends on the antenna geometry. The outgoing Hankel function $H_0^{(2)}(\beta_{TM_0}\rho)$ in (3.21) takes a form similar to (3.18) in the far-field (i.e., when $\rho \gg \lambda$) and represents the 2-D spreading of the field that is guided as surface waves by the substrate.

The simulated electric field distribution of the different waves for the module in the two orthogonal vertical planes containing the main beam is shown in Figure 3.25. The surface wave in air exists primarily near the interface $z = h$ while the space wave dominates the region above some distance from the interface. The wave attenuates exponentially in air away from the interface while it varies as $\cos(\beta_{zd}z)$ in the dielectric, as shown in Figure 3.26. The normalized simulated $|E_z|$ shown is for a distance $\rho = 4.6$ mm away from the array center in the main beam direction ($\phi = 135°$) and is plotted along a line perpendicular to the interface from the ground plane location $z = 0$ to a distance $z = 2.5$ mm above, as shown in Figure 3.25(b). The normalized theoretical $|E_z|$ is calculated from (3.17) and (3.18) using the values listed in Table 3.5. There is a discontinuity of $|E_z|$ at the interface, as predicted by (3.20). The simulated and theoretical $|E_z|$ curves agree well within the dielectric ($z \leq h$) but there is some deviation in air ($z \geq h$). This is due to the presence of the radiation field at and above the interface and other loss mechanisms that are not considered in the theoretical formulation. The exponential decay applies only to the surface wave and the behavior of space wave away from the interface must also be considered.



(a)



(b)

Figure 3.25. (a) Vertical plane ($\phi = 135°$) electric field surface plot of the antenna module at 60 GHz. (b) Electric field distribution in the vertical plane orthogonal to the plane shown in (a) at $\rho = 4.6$ mm from the array center.

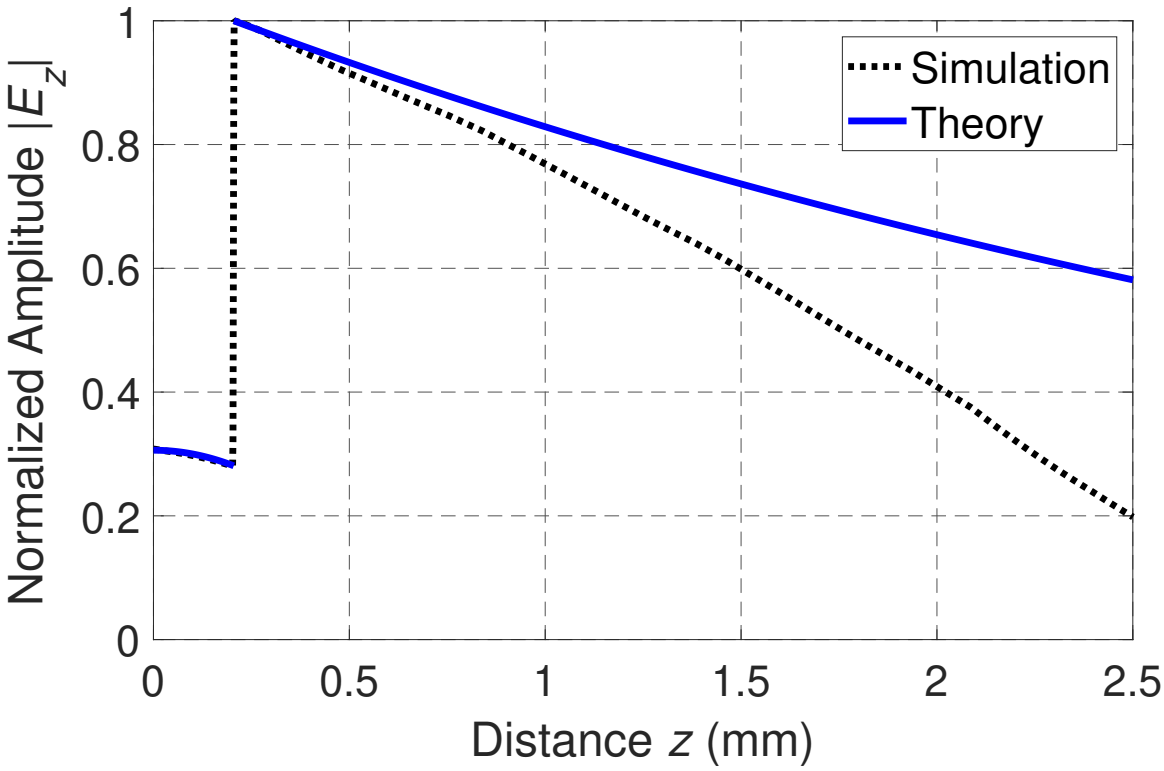


Figure 3.26. Normalized simulated and theoretical $|E_z|$ in the air and dielectric regions as a function of distance z in the vertical direction.

3.6 Gain BW, Beam Squint, and Beam Broadening

The gain variation of the 2 × 2 circular patch planar array along $\phi_0 = +135°$ with and without the Butler matrix/transitions is shown in Figure 3.27. For the case of the standalone array, the elements are excited with equal amplitude and flat phase shifts $\beta_x = +90°$ and $\beta_y = -90°$ over the entire band. There is only 1 dB variation in gain, and therefore, the gain BW of the standalone array is more than 11 GHz.

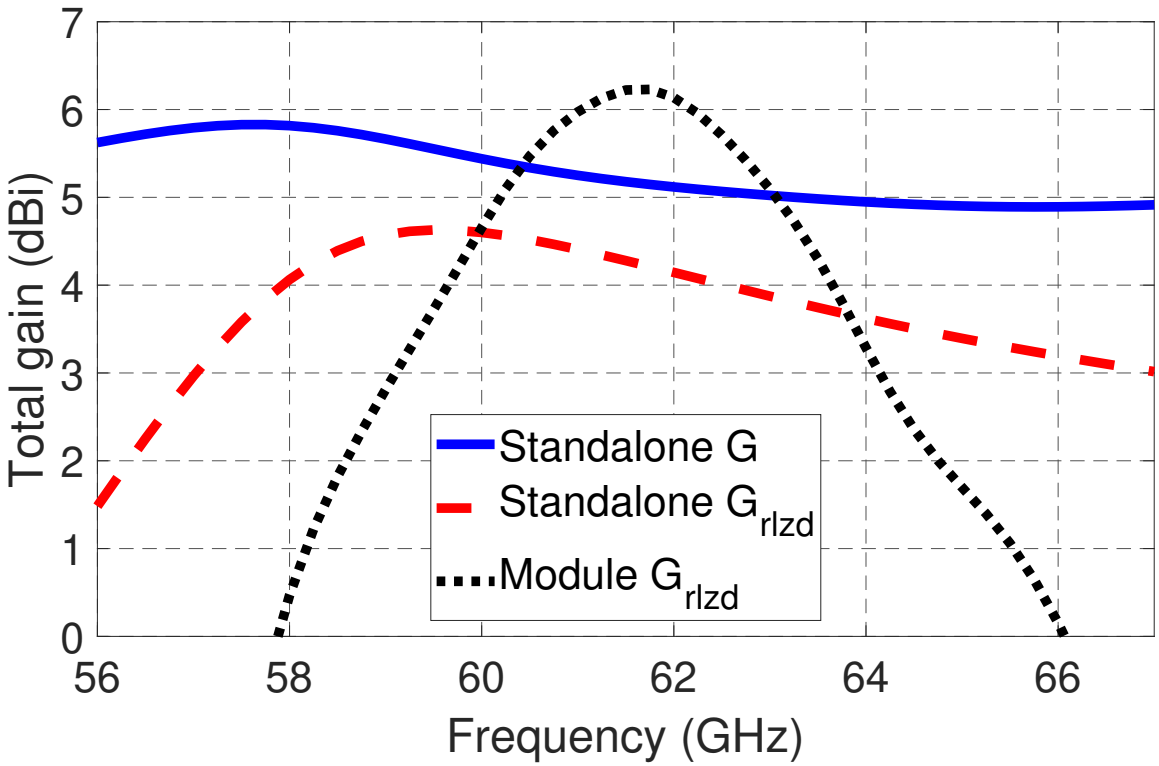


Figure 3.27. Gain response of the planar array along the main beam direction $\phi_0 = +135°$ with and without the Butler matrix. The array without the matrix (standalone) is uniformly excited with flat phase shifts $\beta_x = +90°$ and $\beta_y = -90°$ over the band.

The gain with the reflection (mismatch) losses at the array input taken into account is called the realized gain [21], as captured in (2.71). The *realized gain BW* can be defined using the same 3-dB criterion as the gain BW. It is a more realistic metric of antenna performance since it incorporates both the gain and impedance BW. The realized gain of the array is also plotted in Figure 3.27, from which one can see that there is more variation in gain. Despite this, a realized gain BW of more than 11 GHz is attained. When the planar array is integrated with the Butler matrix and CPW transitions, additional reflection losses are introduced between the blocks and the realized gain BW of the overall antenna module is reduced to 6.75 GHz. The realized gain BWs are listed in Table 3.4. Despite increased losses, the higher gain

of the module in the 60 to 63.5 GHz range is due to the directive radiation from the feed layer and slightly larger substrate. The signal amplitude imbalance and variation at the matrix output can also reduce the BW, in addition to making the radiation patterns more asymmetric.

The gain BW reduction could also be due to some combination of element pattern, array factor and mutual coupling variations. The normalized array factor $\mathrm{AF_n}$ of the planar array, given in (2.3), varies with frequency for constant phase shifts β_x and β_y. It can manifest as beam squint and/or beam broadening in the radiation pattern. Beam squint can limit the gain BW of an array by shifting the main beam away from the LoS. For the planar array, the main beam direction, from (2.4) and (2.5), is given by

$$\phi_0 = \tan^{-1} \frac{\beta_y}{\beta_x} \tag{3.22}$$

The planar array will have a stable main beam as long as the ratio β_y/β_x stays constant with frequency. This is assuming that the element pattern and mutual coupling variations do not dominate. Since the proposed matrix has β_x and β_y responses that are relatively flat [see Figure 3.8(b)] and follow one another, it should only cause negligible beam squint. In Figure 3.20, the radiation patterns at 60 GHz and 67 GHz are shown and there is no noticeable beam squint. The elements are uniformly excited. The phase shifts obtained at the matrix output is used for the 67 GHz case [see Figure 3.8(b)]. The pattern at 67 GHz is broader, more asymmetric and there is 1 dB reduction in gain compared to 60 GHz. Therefore, the slight gain reduction can be attributed to beam broadening.

At 67 GHz, the phase shifts at the matrix output, as seen in Figure 3.8(b), deviate by $\Delta\beta_{x1} = -9.8\%$, $\Delta\beta_{x2} = -2.9\%$, $\Delta\beta_{y1} = +14.8\%$ and $\Delta\beta_{y2} = +21.8\%$ from the required phase $\beta_{req} = \pm 90^\circ$ (given in Table 3.1), calculated as follows:

$$\Delta\beta_{x,y} = \frac{\beta_{x,y} - \beta_{req}}{|\beta_{req}|} \tag{3.23}$$

These phase shift deviations resulted in only 0.5 dB reduction in gain compared

to the no deviation case $\beta_{req} = \pm 90°$ at 67 GHz. Thus, the array gain is not very sensitive to just the phase shift deviations alone. On the other hand, the module shows significant beam squint. Figure 3.28 shows how the angle of the main beam changes as the frequency is increased from 57 to 64 GHz. This could be due to the combination of increased mismatch losses and dispersion of the MS lines of the Butler matrix as the frequency is changed from the design frequency of 60 GHz.

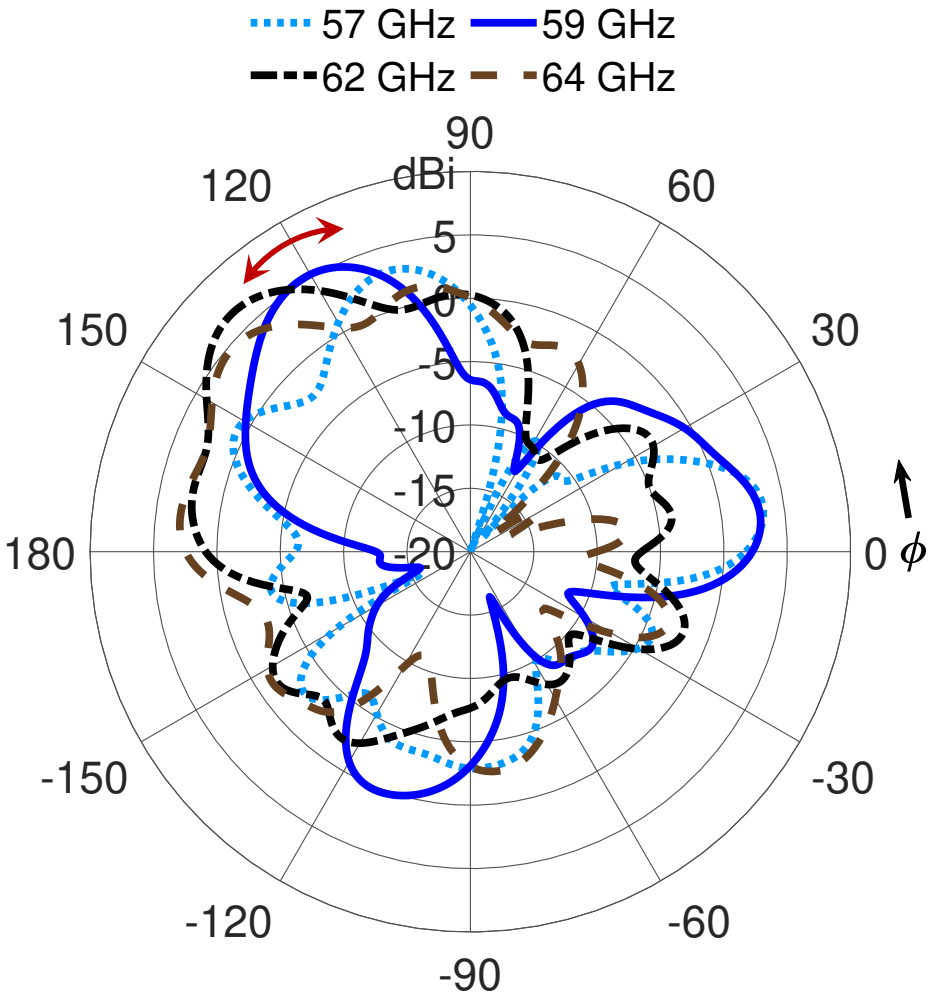


Figure 3.28. $(G_\theta + G_\phi)$ horizontal gain patterns showing the beam squint of the antenna module in the horizontal plane ($\theta = 90°$).

Chapter 4
Chip-to-Chip Communication in MCMC Systems Using the HSSW-I

The antenna modules designed in Chapter 3 are used to realize the HSSW-I and establish chip-to-chip communications. Some of the contents of this chapter have been published in [14, 42]. The HSSW-I is implemented by placing the antenna modules on a common substrate and ground plane. A multiantenna module (MAM) consisting of five antenna modules that emulates interchip communication in MCMC systems is developed and analyzed.

4.1 Realization of HSSW-I Using the Antenna Modules

A specific case of interchip communication between the diagonal neighbors in the MCMC system of Figures 1.8 and 3.1 is considered. To emulate the chip-to-chip communication scenario, five antenna modules are put together to form a larger MAM, as shown in Figure 4.1. The modules are separated by a small interchip diagonal distance of $R = 20$ mm, from one array center to another. All antenna modules are identical to the module in Figure 3.11(b). The substrates and ground planes of each module are connected together to form the HSSW-I layer (with a larger common substrate and ground plane). This allows surface wave coupling to occur between the antenna modules [82,83,85], and improve interchip transmission. This should help to reduce interference between the antenna and the feed layers of the MAM.

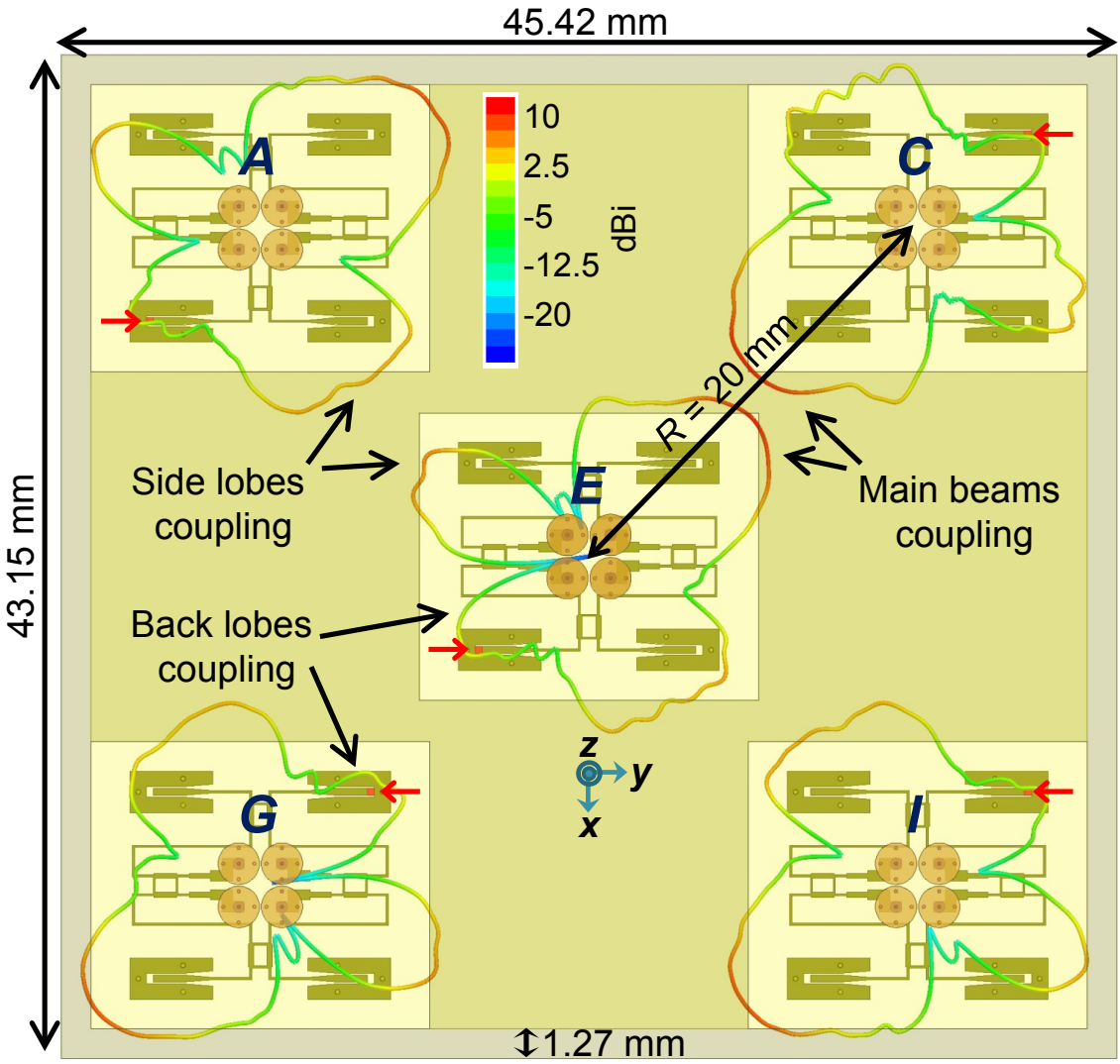


Figure 4.1. MAM 3-D model with five antenna modules. The 60 GHz simulated horizontal gain patterns (dBi) of the modules are overlaid on the MAM [14].

Many pairs of chips are expected to communicate concurrently in MCMC systems to achieve a high degree of parallelism. This can be problematic since the side and back lobes of the radiation patterns of the antennas on the chips can interfere with their neighbors that are also communicating. Consider the beam configuration shown in Figure 4.1, which is representative of a concurrent communication between several chips. The ports (indicated by red arrows) are excited on antenna modules E and C

so that their main beams point at one another. Thus, the pair *E*–*C* is referred to as the communicating pair. At the same time, the ports on modules *A*, *G*, and *I* are also excited so that their main beams point toward neighboring modules other than module *E* (consider the MAM shown in Figure 4.1 is larger and has more modules around it). The radiation from *A*, *G*, and *I* in the direction of *E* contribute to interference and vice versa. The goal is to maximize the radiation between *E*–*C* (communicating pair) while minimizing it between *E*–*A*, *E*–*G*, and *E*–*I* (interfering pairs). The 60 GHz simulated gain patterns of the modules are overlaid on the MAM to show the differences in the radiation coupling between the pairs. The pairs *E*–*A* and *E*–*I* are each coupled through their side lobes and the pair *E*–*G* is coupled through their back lobes. A qualitative analysis of radiation coupling for other beam configurations can be done similarly, using the individual radiation patterns of the modules (see Figure 3.18), their orientation and port excitation. For the interchip communication scheme to work properly, the contention among the modules must be avoided. For example, a contention occurs when modules *A*, *G* and *I* also point their main beam toward *E* (i.e., worst interference scenario). This could be avoided by using few wired control signals on the PCB so that when a pair of modules is communicating, the other modules cannot point their main beam toward the pair and interfere.

Figure 4.2 shows the perspective view of the MAM overlaid with 3-D patterns of each of the modules. It provides a visualization of radiation coupling between the modules as well as to the external surrounding. Since all the diagonal pairs are structurally identical, their transmission coefficients and link budgets will be the same if the main beams are pointed at one another. This ensures an identical link transmission between each communicating pair as the main beam of a module, e.g., *E* is scanned in the four diagonal directions and the other modules also have their main beam pointed toward *E*.

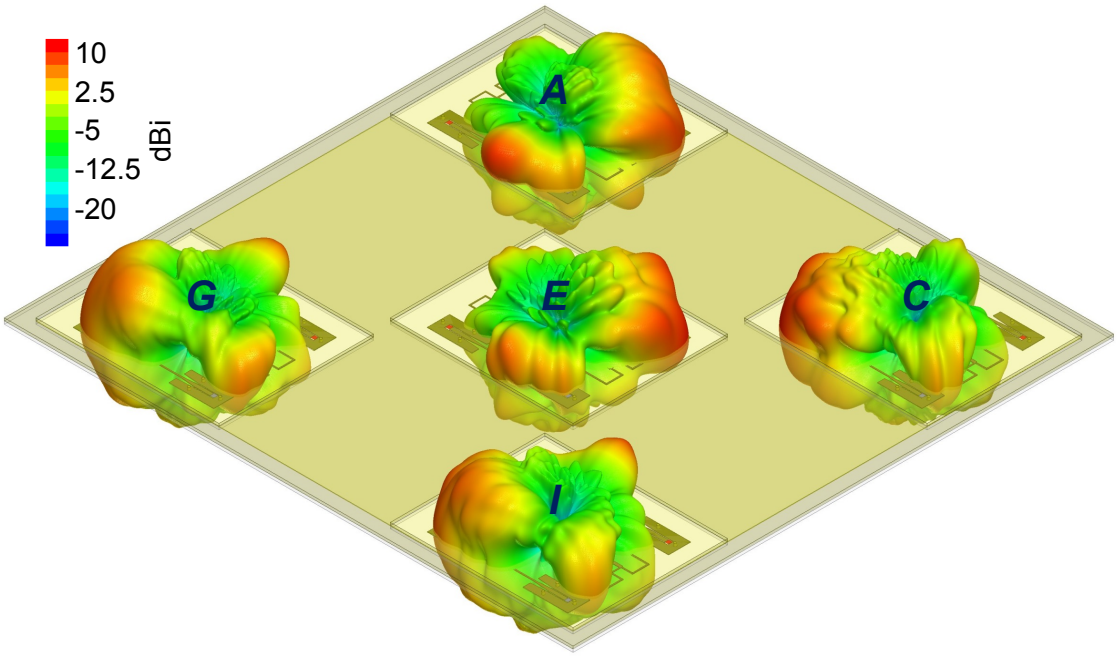


Figure 4.2. The MAM with the simulated 3-D gain patterns (dBi) of the modules overlaid.

4.2 Fabrication Procedure

Industry standard Gerber files and numeric control (NC) drill files are created from the 3-D model of the MAM for fabrication. The fabricated PCB prototypes of the MAM with the view of both the antenna and feed layers are shown in Figure 4.3. The multilayer structures are built up using RO4003C cores, RO4450F prepregs (bondplys), and copper foils through sequential lamination. The core has copper foil pre-bonded onto both sides. At first, the side vias (which are blind vias) are realized. For this the core is mechanically drilled, and the holes are plated-through, filled (with non-conductive epoxy), and plated-shut. Then, resist coating is applied on both surfaces and the layout film is placed on the resist. The surfaces are then exposed to high intensity ultraviolet (UV) light and developed to remove the exposed resist. Then, the antenna layer is etched out from the top foil and the ground plane (i.e., the middle inner layer) is etched out from the lower foil. After that, two sheets of 0.1

mm thick RO4450F prepregs and a copper foil are bonded onto the bottom side of the core using heat and pressure. Two 0.1 mm thick sheets are used to achieve the total thickness of 0.2 mm between the ground plane and the feed layer. During the bonding process, the prepregs melt and flow across the exposed core and the inner layer copper traces, creating a strong bond in the subsequent cooling phase. The resulting multilayer structure is then mechanically drilled, plated-through, filled (with non-conductive epoxy), and plated-shut to form the center feed vias. After that, the ground vias (which are also blind vias) are laser drilled and filled with copper. The laser drill process results in tapering of the via diameter with depth, which is incorporated in the HFSS 3-D model of the antenna module, as shown in Figure 3.11(a). The via aspect ratio h/a_{g1}, i.e., depth to diameter is less than one, which ensures that the vias can be properly plated and filled to establish good connection between the layers. Finally, the feed layer is etched out from the bottommost copper foil of the prepreg after resist coating, exposure, and development of the surface.

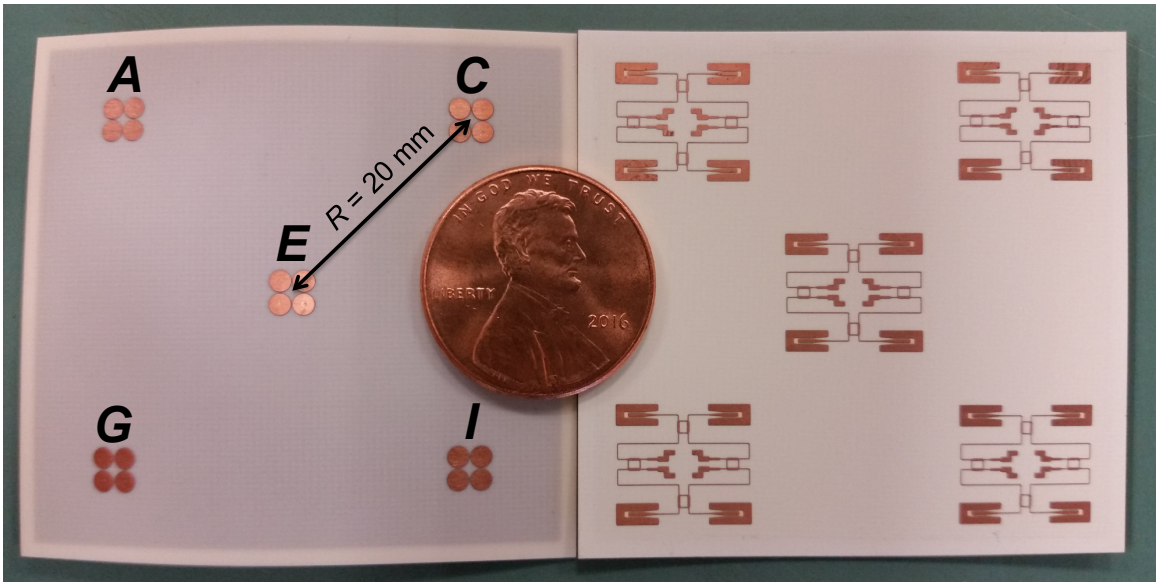


Figure 4.3. Fabricated PCB prototypes of the MAM, with five antenna modules on each, are laid side by side to show the antenna and feed layers. A US penny is placed on top of the boards for size reference.

4.3 Measurement Setup and Thru-Reflect-Line (TRL) Calibration

The S-parameter measurements on the MAM are made using 250 μm pitch GSG probes, connected to Agilent's 67 GHz E8361A performance network analyzer (PNA). An off-chip TRL calibration is performed using the precision calibration standards on an impedance standard substrate (ISS). The ISS with the standards is shown in Figure 4.4. The calibration characterizes the combined non-ideal behavior of the PNA, cables, connectors, and probes by measuring the known and partially known standards and corrects the measurement so that only the device-under-test (DUT) characteristics can be later isolated [86].

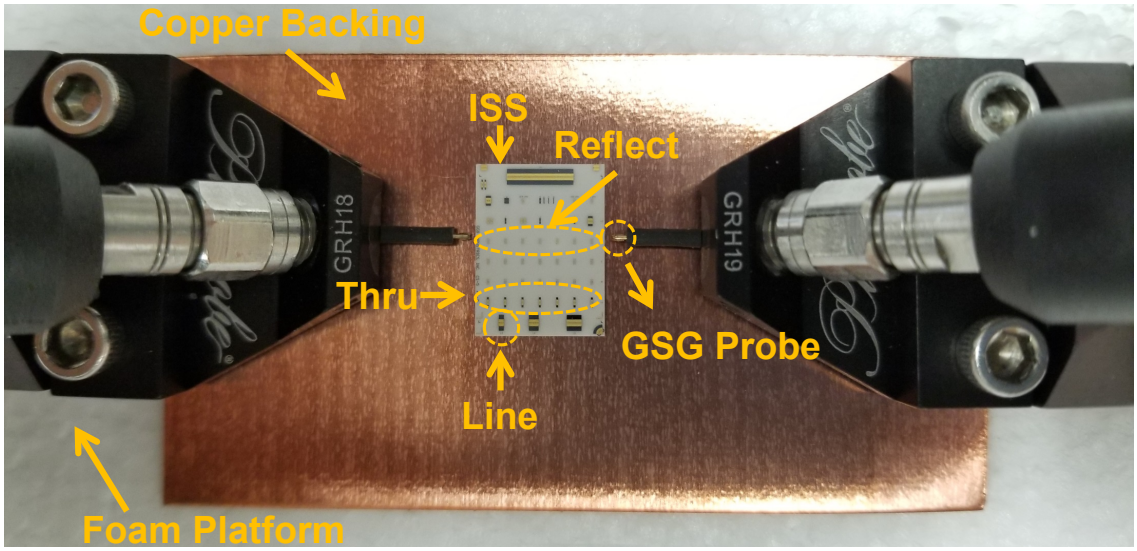


Figure 4.4. ISS with precision TRL calibration standards.

The differences in pad layout and dielectric constant between the ISS and DUT substrate usually only results in measurement errors in phase and delay. The magnitude measurements such as the return and insertion losses are not affected [86]. On the other hand, an on-chip TRL calibration is more accurate, at least on paper, since launch differences can be minimized by creating standards on the DUT substrate with the same pad layout. However, using PCB techniques, precise thru and

line standards are hard to fabricate on the DUT substrate especially when the trace spacing is small, as is the case for the MAM to be tested [trace spacing $g_1 = 0.08$ mm = 3 mil, see Table 3.3 and Figure 3.11(b)]. The surface roughness of the traces is also hard to control with PCB fabrication and can affect the quality of the line standards especially around 60 GHz. Therefore, an off-chip TRL calibration on ISS is pursued.

The PNA is turned ON and allowed to warm up for few hours to let it settle to its thermal equilibrium before performing the calibration. The measurement sweep is made from 56 to 67 GHz in 0.01 GHz steps. Each frequency point in the sweep is stepped meaning that there is a delay before the response is measured and before the PNA source is tuned to a new frequency point. This allows the DUT response to settle and results in higher data acquisition accuracy. A low IF BW of 100 Hz is used for higher dynamic range calibration and sweep averaging is enabled to reduce the effects of random noise on the measurements. The measurement setup details are summarized in Table 4.1.

Table 4.1. Measurement equipment, calibration, and settings

Description	**Specification**
Network analyzer	E8361A PNA (Agilent)
Probes	67A-GSG-250-DP (GGB)
PNA/probe connectors	1.85mm/V
Calibration ISS	CS-5 (GGB)
Calibration method	TRL
Thru length	150 μm
Reflect type	Open
Line length	500 μm
ISS propagation velocity	$0.442c_0$
Sweep type	Linear: 56 to 67 GHz
Sweep step	0.01 GHz
Sweep setup	Stepped
Sweep time	15 s
Port power	-6 dBm
IF BW	100 Hz
No. of sweeps averaged	4

The open pads on the ISS are probed to get the data for reflect standard during TRL calibration. The ISS calibration coefficient $C_0 = 6.5$ fF, which models the parasitic capacitance of the open pads, is taken into account in the TRL calibration algorithm (supplied with the PNA), to further improve the reflect calibration accuracy. The reflect standard must have a high reflection coefficient with the phase known within $\pm 90°$. The impedance of the open pads Z_p is given by

$$Z_p = \frac{1}{j2\pi f C_0} \tag{4.1}$$

The reflection coefficient of the open pads Γ_p can be calculated as

$$\Gamma_p = \frac{Z_p - Z_0}{Z_p + Z_0} \tag{4.2}$$

where Z_0 is the characteristic impedance of the thru and line standards, usually 50 Ω. Using (4.1) in (4.2), $\Gamma_p \approx 1\angle -14°$ is calculated at 60 GHz, which satisfies the magnitude and phase criteria for a reflect standard in TRL calibration [87]. The crosstalk (signal coupling) between the probes, when one probe is on an open pad and the other probe is on a nearby open pad, can affect the measurement accuracy. Even if the crosstalk is initially taken into account in the calibration, when the probes are moved after calibration to measure the DUT, the crosstalk changes and the measurement can be somewhat affected. The high dielectric constant of the ISS usually helps to limit the probe crosstalk in air. Probe placement and contact variations can also cause small errors in measurement. Furthermore, the calibration standards on the ISS should be sufficiently separated to reduce unwanted coupling between adjacent structures during calibration.

To get the data for thru and line standards, the lines of physical lengths $L_t = 150$ μm and $L_l = 500$ μm, respectively, are probed on the ISS. These physical lengths are specified to be suitable for TRL calibration from 25 GHz to 110 GHz which more than covers the measurement range considered and a multi-line TRL (ML-TRL) calibration is not required. The lines can be considered to be in an effective

medium formed by the ISS and the air. The velocity of propagation of signal in this medium is provided by the manufacturer and is $v_p = 0.442c_0$ (where c_0 is the velocity of light in air). This enables thru and line delays to be calculated as

$$\tau_{t,l} = \frac{L_{t,l}}{v_p} \tag{4.3}$$

These delays are required by the TRL algorithm. The phase difference $\Delta\theta$ between the line and thru standard is given by [87]

$$\Delta\theta(f) = \frac{2\pi f}{v_p}(L_l - L_t) \tag{4.4}$$

Within the frequency range of measurement, the phase difference $\Delta\theta(f)$ should satisfy the following TRL phase criterion [87]:

$$20^\circ < \Delta\theta(f) < 160^\circ \tag{4.5}$$

For the measurement range 56 GHz $\leq f \leq$ 67 GHz, using (4.4), $53.2^\circ \leq \Delta\theta(f) \leq 63.7^\circ$ is calculated, and the criterion in (4.5) is indeed satisfied for all frequencies within the band. After the TRL routine is run, the calibration is checked and verified by remeasuring the S-parameters of the same reference standards as well as measuring other standards (e.g., short bars) and line lengths provided on the ISS.

4.4 Simulation and Measurement of Reflection and Interchip Transmission Coefficients

The measurement setup with the GSG probes is shown in Figure 4.5(a). The MAM is placed on a thick foam platform (no metal chuck underneath) for stability during measurements. The feed layer is facing up to allow for probing and the antenna layer faces down. Without the foam, the antenna layer would be shorted out by the chuck. The dielectric constant of foam is close to one and thus emulates air. Therefore, it should only cause minor perturbation in the near-field of the antenna modules and hence the measurements [70, 88]. A view of the CB-CPW line being probed

through the lens of a microscope is shown in Figure 4.5(b). Before performing the TRL calibration, a copper backing plate is used underneath the ISS to serve as the ground plane and then placed on the foam platform, as shown in Figure 4.4. Then, the calibration standards are probed, and the calibration is verified before proceeding with the measurement. The reflection coefficient of the thru standard is less than -45 dB across the measurement band indicating a good calibration. This also sets the noise floor for reflection measurements. The simulated and measured reflection coefficients at a CB-CPW input of the antenna module E are shown in Figure 4.5(c).

The measured reflection coefficient curve is shifted higher in frequency but other than that, a good agreement with the simulated curve is seen. The measured and simulated impedance BWs are 7.57 and 9.75 GHz respectively, using the $|S_{11}| \leq -10$ dB criterion. The antenna module is able to achieve the broad BW because of good impedance matching between the individual blocks, namely the CB-CPW transitions, the Butler matrix, and the circular patch planar array. Specifically, the use of the linear taper to reduce impedance mismatch at the CB-CPW/MS interface and the use of the common ground plane to decouple the antenna layer from the feed layer provided seamless integration with no significant performance degradation. The reflection coefficient is shown all the way down to 53 GHz in Figure 4.5(c). At 55 GHz, the measured value goes up to -4 dB and up to -7 dB as it approaches 67 GHz. These indicate that the low reflection coefficient measured from 58 to 66 GHz is mostly due to good impedance matching and not due to high substrate and conductor losses.

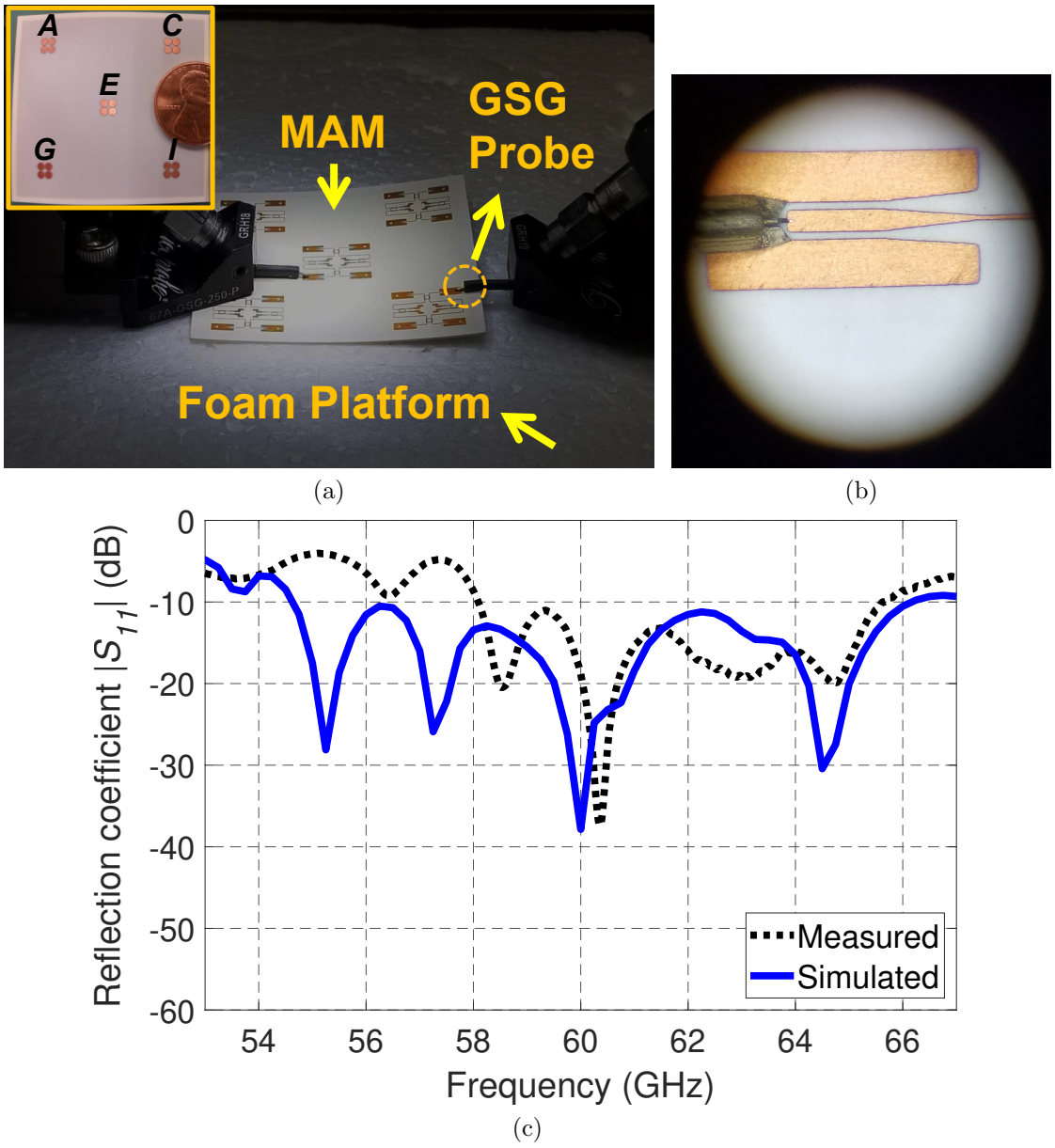


Figure 4.5. (a) Measurement setup of the fabricated MAM prototype [14]. (b) Microscope view of the GSG probe on the CB-CPW line. (c) Reflection coefficient (dB) of the antenna module E on the MAM [14].

The transmission coefficient S_{21} (total) between any two modules on the MAM is found by running the full-wave simulation of the 3-D model in Figure 4.1. The transmission coefficient of the thru standard is a flatline near 0 dB, which indicates

a good calibration. The open probes when separated by 14 mm had a transmission coefficient of less than -80 dB in the entire band and this sets the noise floor for transmission measurements. The transmission coefficients between *E*–*C*, *E*–*I*, *E*–*A*, and *E*–*G* are measured and simulated. The results in Figure 4.6 show that the transmission $|S_{CE}|$ for the communicating pair *E*–*C* is generally higher than the transmission $|S_{IE}|$, $|S_{AE}|$, and $|S_{GE}|$ for the interfering pairs *E*–*I*, *E*–*A*, and *E*–*G* across the band, for both measured and simulated values, respectively. This is important in order to keep the signal levels on the wireless link higher than the interference levels and maintain a low BER on the channel. The differences in the levels of $|S_{CE}|$, $|S_{IE}|$, $|S_{AE}|$, and $|S_{GE}|$ are due to differences in the gain (i.e., main, back and side lobes) of *E* in the direction of *C*, *I*, *A*, and *G*. The main lobe level must be maximized while minimizing the back and SLLs in order to maximize the signal-to-interference ratio (SIR) and the throughput.

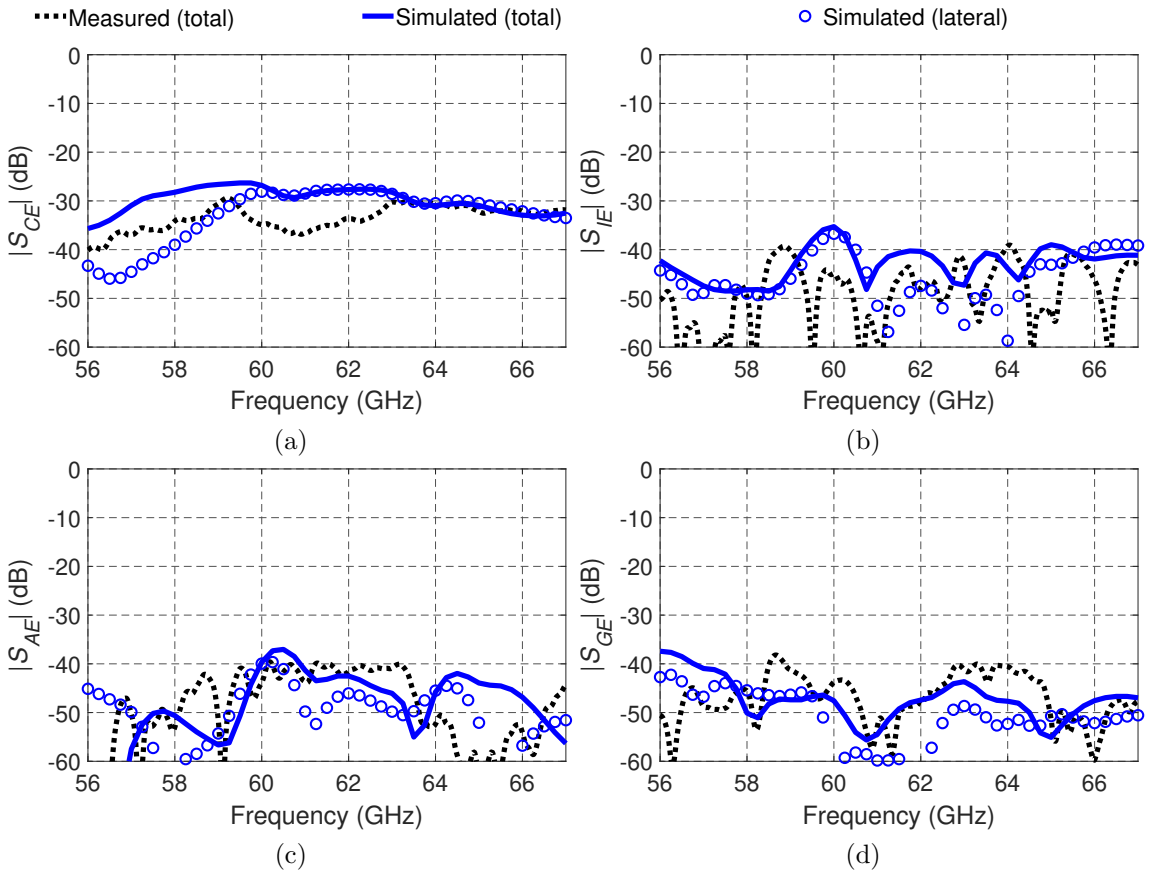


Figure 4.6. Measured and simulated transmission coefficients (dB) between the antenna modules on the MAM [14]. (a) $|S_{CE}|$. (b) $|S_{IE}|$. (c) $|S_{AE}|$. (d) $|S_{GE}|$.

A detailed link budget analysis that takes into account interference and noise sources in the given scenario to estimate the SNIR (and hence the main and side lobe levels) required to achieve a given interchip data rate at a given BER for a particular modulation scheme used is presented in Section 4.6. Generally, the measured transmission is somewhat lower than the simulated transmission across the band for all pairs in Figure 4.6. This is predominately due to higher dielectric and conductor losses than accounted for in simulation. Other factors for the deviation could be the non-ideal manufacturing process and the high tolerances associated with PCB fabrication, both of which results in a prototype that deviates from an optimized design. The PCB prototypes in Figure 4.3 are not perfectly flat. Specifically, the

boards have curvature with each of their four corners in the same plane (bow condition). The boards bow because of asymmetrical stackup of the core, prepregs and copper distribution around the center of the PCB, as shown in Figure 3.11(a). The boards are only 0.4 mm thick, which could have also contributed to bowing. Bowing can cause both vertical and horizontal misalignment between the antenna modules on the MAM, which can change the LoS antenna gains and thus affect transmission measurements. At 60 GHz, the surface roughness of the conductors can result in increased losses and other performance deviations. This could explain the small ripples seen in the measured curves. Still, there is good agreement in trend with slight shift in frequency between the measured and simulated results. The manufacturing deviations are considered in Chapter 5. The simulated and measured results of the MAM when placed on a foam backing with the metal chuck underneath are presented in Appendix D.

4.5 Link Decomposition and Transmission BW

The total transmission $|S_{21}|^2$ between any two antenna modules on the MAM is the sum of lateral space wave $|S_{21}^l|^2$ and surface wave $|S_{21}^s|^2$ components as follows [60]:

$$|S_{21}|^2 = |S_{21}^l|^2 + |S_{21}^s|^2 \tag{4.6}$$

The S_{21}^l can be estimated by performing another full-wave simulation of the MAM but after removing the intervening substrate and ground plane between the modules, as shown in Figure 4.7. All antenna modules are identical to the one shown in Figure 3.11(b) but without the 1.27 mm substrate extension on their sides.

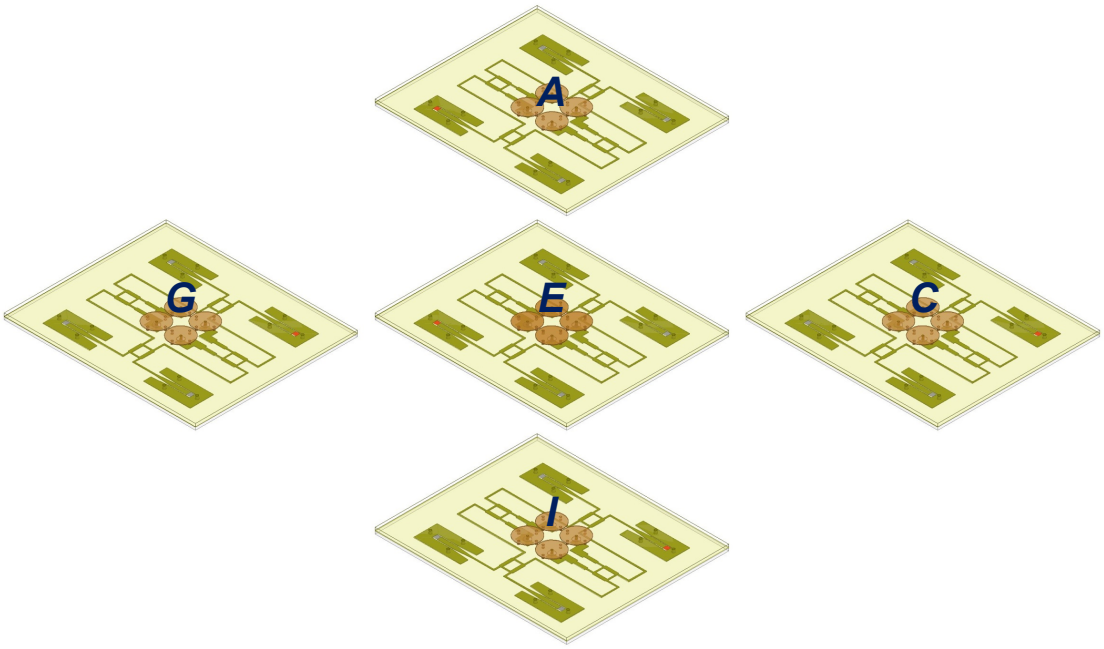


Figure 4.7. MAM 3-D model with the intervening substrate and ground plane removed between the modules. Full-wave simulation of this model yields an estimate for lateral space wave component.

By doing this, the modules are physically separated from one another. Therefore, the lateral space wave component S_{21}^{l} can be isolated since there is no direct surface wave coupling. The $|S_{21}^{l}|$ (lateral) for the pairs E–C, E–A, E–G, and E–I are shown in Figure 4.6. Diffraction effects at the substrate/ground plane edges of the modules will introduce some errors in the estimation of $|S_{21}^{l}|$ but the thin nature of the substrate should help to keep such errors small. The surface wave component $|S_{21}^{s}|$ can then be estimated by subtraction [60], using (4.6), as is shown later in Figure 4.16. In this way, the total transmission can be decomposed into its lateral space and surface wave components.

In Figure 4.6(a), comparing the simulated $|S_{CE}|$ (total) and $|S_{CE}^{l}|$ (lateral) transmission curves, the contribution of surface wave coupling can be seen to occur at and below 60 GHz. Thus, the surface waves have helped to increase transmission below 60 GHz. As much as 11 dB improvement in transmission can be seen at 58 GHz.

The surface wave coupling has also helped to improve the transmission flatness below 60 GHz. On the other hand, above 60 GHz, the transmission contribution is mostly from the lateral space waves.

As introduced in Section 1.9.1, applying the 3-dB criterion to the $|S_{CE}|$ (total) curve in Figure 4.6(a), the simulated transmission BW of the proposed HSSW-I is 6.25 GHz. The BW of the link considering only the lateral space wave coupling $|S_{21}^{l}|$ is reduced to 4 GHz. Therefore, the surface waves have significantly improved the transmission BW. They can be useful to maintain link power especially at larger distances. To verify this, another set of simulation between the pair E–C with their separation R increased to 30.8 mm is conducted and the link decomposition technique is applied. About 3 dB improvement in transmission is seen at and above 60 GHz, and more than 11 dB at 58 GHz, due to the surface waves, as is shown later in Figure 4.15(b).

One disadvantage of surface wave coupling is that the interference levels have also increased at certain frequency points, as shown in Figure 4.6(b), (c), and (d). However, since the increase in signal transmission is more consistent throughout the band, the surface waves should help to improve the overall SNIR of the link.

A simplified link model that takes into account both the space and surface wave coupling between any two identically oriented antenna arrays in the far-field is introduced in [82]. As the separation R increases, the relative contribution of surface waves increases. This is because the surface waves decay at a slower rate i.e., $1/R$ compared to $1/R^4$ for the lateral space waves. The link models are useful to reduce the number of simulations and to perform quick link analyses at the network layer, once the link coefficients are determined. Recently in [83, 85], the link coefficients for two fixed-beam arrays at 60 GHz using the least-squares method is estimated. A new link model for the switched-beam arrays is introduced in Section 4.8. The simulated data obtained from the link decomposition technique is used for to determine the link coefficients of this model.

The features of the antenna module presented in this dissertation are compared with other 60 GHz switched-beam modules (also fed with Butler matrix) in Table 4.2. The module developed has the smallest footprint and provides the 360° angular coverage in the four diagonal directions, which is not seen in the other works. Smaller antennas allow the chip-antenna package size to be reduced. So, the packages can be placed closer to one another and thus minimize the chip-to-chip distances.

Table 4.2. Feature comparison of 60 GHz switched-beam antenna arrays fed with Butler matrix

Ref.	**Array Type**	**Scanning Coverage**	**No. of Beams**	**Butler Matrix**	**Area (mm^2)**
[50]	2×4 Stacked Patches	Broadside	8	MS	24×24
[56]	1×8 ME Dipoles	Endfire (180°)	8	SIW	63×30 (est.)
[57]	2×2 ME Dipoles	Broadside	4	SIW	58×42 (est.)
This Work	2×2 Circular Patches	Endfire (360°)	4	MS	15×17

4.6 Link Budget Calculations

Intrachip and interchip data transfer play a key role in determining the performance of many-core systems [11] like the MCMC. Such data communications must be high throughput with low latency in order to realize a fast computing system [10]. A 60 GHz non-wired interconnect can offer multi-Gbps throughput required for intrachip and interchip communication in high performance MCMC systems [9,13,14,71]. The link budget of the communication scenario shown in Figure 4.1 is analyzed at a system level to understand how antennas, transceivers, interconnections, noise, and interference sources play a role in determining the achievable data rate.

First and foremost, the SNIR available at the RX end dictates the order and type of digital modulation schemes that can used for a low BER communication. The modulation, in turn, determines the data rate that can be achieved between the antennas. For the MCMC communication scenario shown in Figure 4.1, the average transmission $|S_{CE}|^{avg}$ determines the signal power S as

$$S(\text{dBm}) = |S_{CE}|(\text{dB}) - 2L_{\text{SP4T/FC}}(\text{dB}) + P_t(\text{dBm}) - \text{LM (dB)} \tag{4.7}$$

where $L_{\text{SP4T/FC}}$ is the cascaded SP4T switch [78] and flip-chip power loss factor, and the factor 2 accounts for losses at both the TX and RX ends, LM is the average link margin loss factor to allow for additional mismatch and implementation losses [29], and P_t is the TX output power supplied to the input of the TX antenna. The key components that are part of the interchip link are illustrated in Figure 4.8.

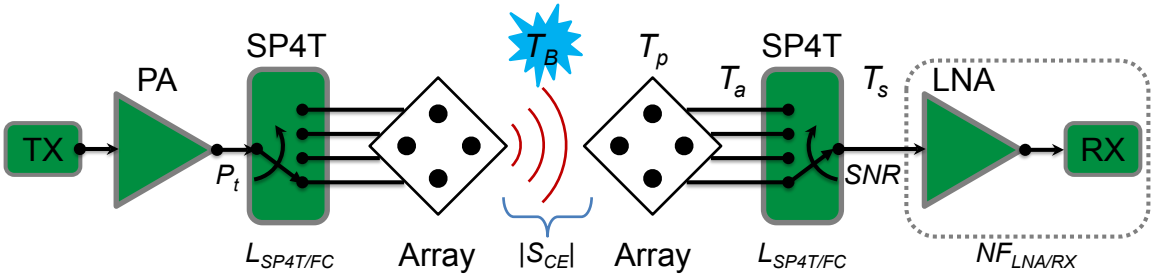


Figure 4.8. Block diagram of the interchip link between the TX and RX using the 2×2 circular patch antenna modules.

The maximum output power that a TX antenna is allowed to radiated is usually given in terms of the EIRP. It represents the power radiated by an equivalent isotropic antenna and is given by

$$\text{EIRP} = P_t G_t \tag{4.8}$$

where G_t is the gain of the TX antenna. Note that G_t and G_r do not appear in (4.7) since the antennas are not in the far-field of one another. The gains of both TX and RX antennas (which will be different from the gains in the far-field) as well as LoS path loss are already incorporated in the transmission coefficient $|S_{CE}|$.

The maximum allowed EIRP for unlicensed usage in the US is $\text{EIRP}_{\max} = 40$ dBm, which is set by the FCC [50]. However, this is not yet a limitation as the current state-of-the-art 60 GHz CMOS TX can only produce $P_t = 14$ dBm [47]. If this TX is used with the antenna module developed in this dissertation (which has $G_t = 5.3$ dBi), then for the communication scenario considered, EIRP = 19.3 dBm from (4.8), and hence, $\text{EIRP} < \text{EIRP}_{\max}$ and the link will be FCC compliant in the far-field region.

4.6.1 Noise Sources

In the absence of the interference sources, the noise picked up by the RX antenna must be considered for a realistic link budget estimation. The increased atmospheric loss at 60 GHz means that the antenna sees a constant background temperature $T_B = 290$ K [24] (regardless of the elevation angle θ and hence the gain pattern of the antenna) that acts as an external noise source. The presence of the ground plane in HSSW-I minimizes the amount of background noise picked up by the antenna from high temperature CMOS electronics underneath and prevents T_B from increasing. In addition to the constant background noise, thermal noise will be generated internally due to the losses within the antenna. The resulting noise temperature T_a seen at the antenna terminals is

$$T_a = e_{mod} T_B + (1 - e_{mod}) T_p \tag{4.9}$$

where T_p is the antenna physical temperature. The signal received by the RX antenna is attenuated due to the losses in the SP4T switch and flip-chip interconnection (both at physical temperature T_p) before it reaches the RX. These losses will also introduce their own thermal noise [89] by increasing the system noise temperature T_s seen at the cascaded LNA and RX terminals (see Figure 4.8), which is given by

$$T_s = T_a + (L_{\text{SP4T/FC}} - 1) T_p + L_{\text{SP4T/FC}} T_{\text{LNA/RX}} \tag{4.10}$$

where $T_{\text{LNA/RX}}$ is the cascaded RX noise temperature and is related to its cascaded NF i.e., $\text{NF}_{\text{LNA/RX}}$ by

$$T_{\text{LNA/RX}} = (\text{NF}_{\text{LNA/RX}} - 1)T_0 \tag{4.11}$$

where $T_0 = 290$ K is the standardized temperature.

The average noise power N at the input terminals of the cascaded LNA/RX can then be calculated as

$$N(\text{dBm}) = 10\log_{10}(k_B T_s \times 1000) + 10\log_{10}(\text{BW}) \tag{4.12}$$

where BW is the RX BW and $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann's constant. The various link parameters with the components involved is depicted in Figure 4.8. Other types of noise when significant should also be considered.

From (4.7) and (4.12), the SNR at the cascaded RX input (see Figure 4.8) can then be calculated as

$$\text{SNR (dB)} = S(\text{dBm}) - N(\text{dBm}) \tag{4.13}$$

The TX noise and distortion do not generally need to be considered in the link analysis since they are usually attenuated below the RX noise floor due to the path loss [47]. Table 4.3 lists the values and estimates of various link parameters associated with the link budget calculation.

Table 4.3. Link budget for the HSSW-I

Parameter	**Value**
Frequency span	57.24 to 65.88 GHz
Distance	20 mm
TX/RX antenna gain	5.3 dBi
RX BW (four channels)	8.64 GHz
TX power P_t	14 dBm [47]
Loss factor $L_{\text{SP4T/FC}}$	5 dB [29, 78]
Link margin LM	8 dB [47]
$T_a = T_B = T_p$	290 K
T_s	2900 K
Background + thermal noise (N)	-64.6 dBm
Cascaded RX $\text{NF}_{\text{LNA/RX}}$	5 dB [47]

The SNR as a function of frequency is shown in Figure 4.9, which is calculated using the simulated and measured $|S_{CE}|$, given in Figure 4.6.

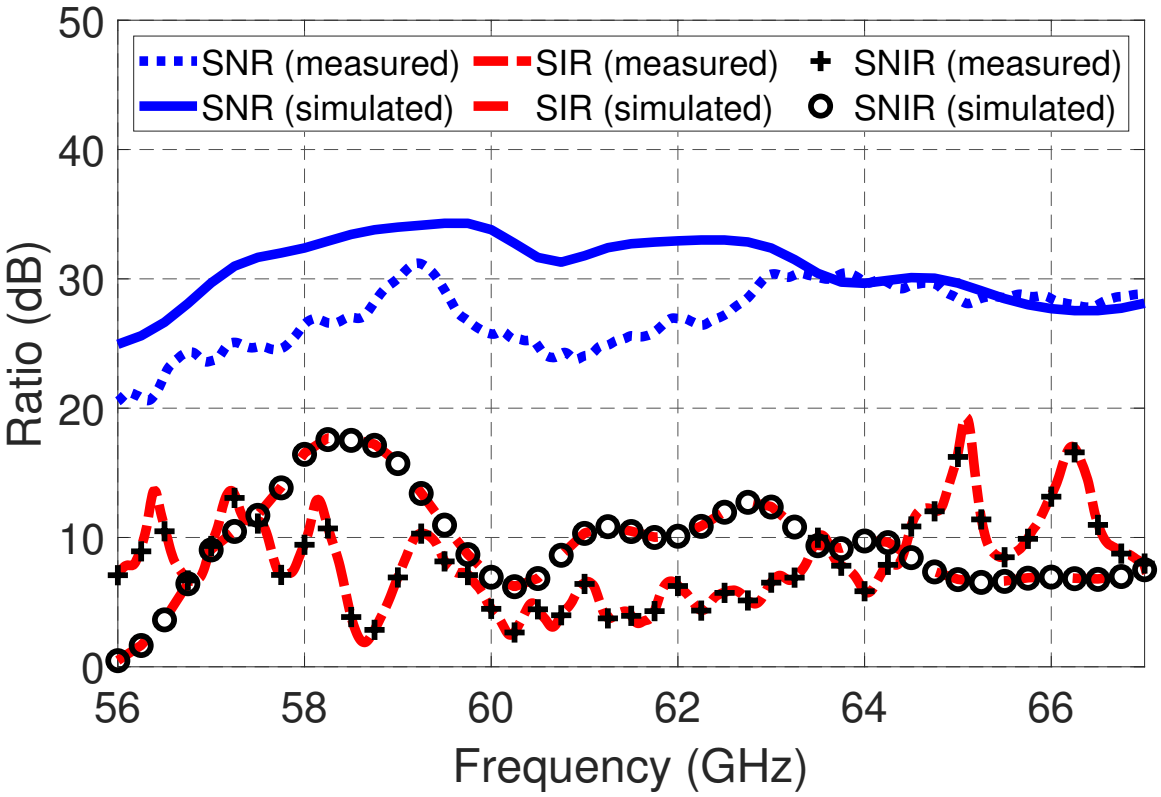


Figure 4.9. SNR, SIR and SNIR calculated using simulated and measured transmission coefficients.

The IEEE 802.11ad specifies a usable RX BW of 1.76 GHz per channel, as is shown in Figure 1.14. The four channels of the standard span from $f_1 = 57.24$ GHz to $f_2 = 65.88$ GHz with the total usable BW of $4 \times 1.76 = 7.04$ GHz. For link budget calculations, the average $|S_{CE}|$ (in dB) within the band can be calculated as follows:

$$|S_{CE}|^{avg}\ (\text{dB}) = 10\log_{10}\left(\frac{\int_{f_1}^{f_2}|S_{CE}(f)|^2 df}{f_2 - f_1}\right) \tag{4.14}$$

Equation (4.14) is just the negative of the link metric L^f_{link} defined in (1.12). The L^f_{link} for the communicating pair calculated using simulated and measured $|S_{CE}|$ are

listed in Table 4.4. The average SNR within the band can be calculated using $|S_{CE}|^{avg}$ in (4.7) and substituting it in (4.13). The values obtained using both simulated and measured $|S_{CE}|^{avg}$ are also listed in Table 4.4.

Table 4.4. Average link loss L^f_{link} and SNR within the IEEE 802.11ad band

Type	$\boldsymbol{L^f_{link}}$	**SNR**
Measured	32.6 dB	28 dB
Simulated	28.5 dB	32.1 dB

The average SNR, both measured and simulated, exceed the minimum required SNR i.e., $\text{SNR}_{\text{min}} = E_b/(N_0 + I_0) + 10\log_{10} N_b = 18.8 + 10\log_{10}(6) = 26.6$ dB for 64-QAM modulation at BER $= 10^{-6}$ (see Figure E.1), and thus, a raw data rate of $4 \times 1.76 \times \log_2(64) = 42.24$ Gbps is achievable, using the proposed HSSW-I with four-channel bonding (i.e., multi-channel operation). Higher order modulation support with channel bonding can push the achievable data rate even higher.

4.6.2 Interference Sources

If the antennas I, A, and G are also communicating to other surrounding chips, as depicted in Figure 4.1, then they act as interference sources for the receiving antenna E. The interference power I can be calculated as

$$I(\text{dBm}) = |S_{intf}|(\text{dB}) - 2L_{\text{SP4T/FC}}(\text{dB}) + P_t(\text{dBm}) - \text{LM (dB)} \tag{4.15}$$

where $|S_{intf}|$ is the total interference transmission coefficient, obtained by adding the transmission coefficients of all the interference sources as

$$|S_{intf}|(\text{dB}) = 10\log_{10}\left(|S_{IE}|^2 + |S_{AE}|^2 + |S_{GE}|^2\right)(\text{dB}) \tag{4.16}$$

The calculated $|S_{intf}|$ is shown in Figure 4.10, obtained using simulated and measured data shown in Figure 4.6.

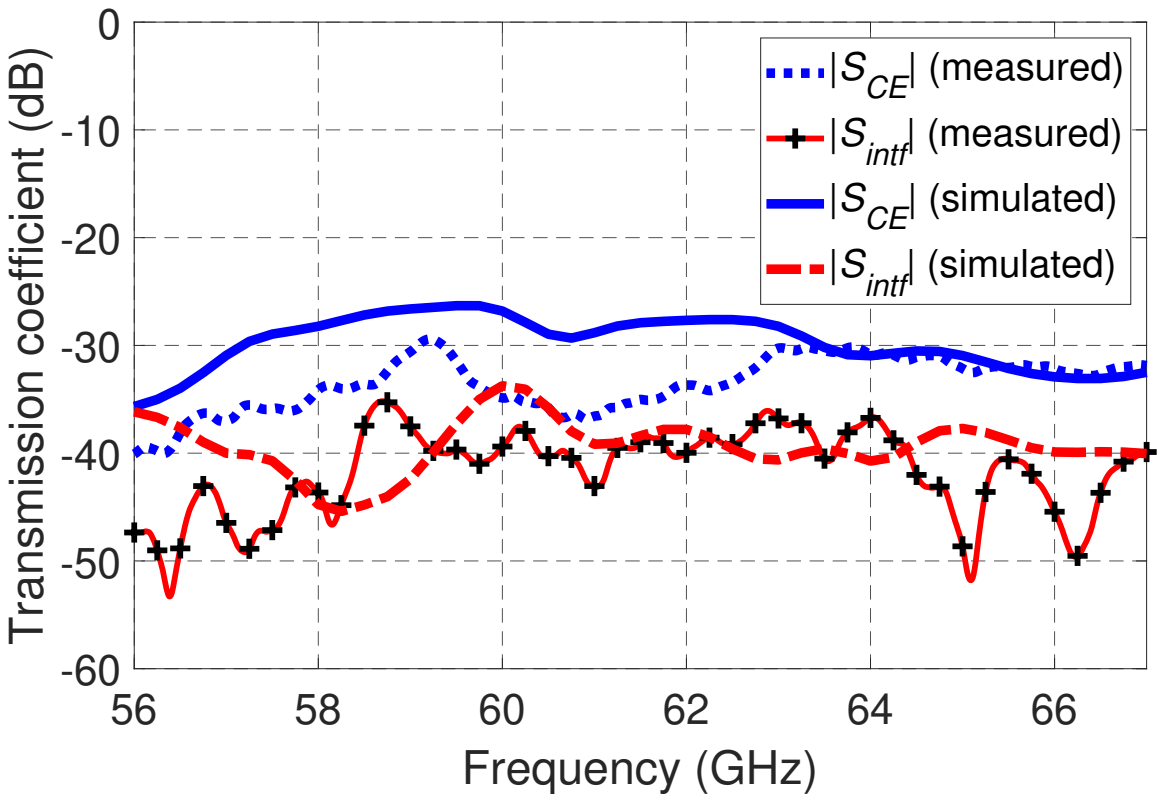


Figure 4.10. Interference coefficient $|S_{intf}|$ (dB) calculated using simulated and measured data. $|S_{CE}|$ curves are repeated here again for reference and they have higher levels than $|S_{intf}|$ curves.

It is interesting to see that the loss mechanisms that reduce the signal power also reduce the interference power, unlike that of noise power, which always increases with losses. The noise power can be neglected if the interference power is significantly higher. From (4.7) and (4.15), the SIR (i.e., ignoring noise) can be calculated as

$$\begin{aligned} \text{SIR (dB)} &= S(\text{dBm}) - I(\text{dBm}) \\ &= |S_{CE}|(\text{dB}) - |S_{intf}|(\text{dB}) \end{aligned} \tag{4.17}$$

The SIR can be gauged from the difference of $|S_{CE}|$ and $|S_{intf}|$ curves in Figure 4.10. The calculated SIR over the whole band is shown in Figure 4.9. The SIR is independent of P_t, $L_{\text{SP4T/FC}}$, and LM because same input power, switch interconnections and link margins are assumed for all the antenna pairs on the MAM module

shown in Figure 4.1.

The SNIR can be calculated as

$$\text{SNIR (dB)} = S(\text{dBm}) - 10\log_{10}(N + I)(\text{dBm}) \tag{4.18}$$

The calculated SNIR is also shown in Figure 4.9, which is obtained using the simulated and measured transmission coefficients, shown in Figure 4.6. The average SIR and SNIR within the IEEE 802.11ad band can be calculated from (4.17) and (4.18) respectively, using the averages $|S_{CE}|^{avg}$ and $|S_{intf}|^{avg}$. They are listed in Table 4.5. From Tables 4.4 and 4.5, one can deduce that the average interference power is more than 21 dB higher than average noise power and thus will dominate noise over the entire band. Therefore, SIR $\approx$ SNIR, in Figure 4.9.

Table 4.5. Average SIR/SNIR within the IEEE 802.11ad band

Type	**SIR/SNIR**
Measured	7 dB
Simulated	10.2 dB

The minimum required SNIR for various modulation schemes are given in Appendix E. The average SIR/SNIR, both measured and simulated, exceed the minimum required SNR i.e., $\text{SNR}_{\text{min}} = E_b/(N_0 + I_0) + 10\log_{10} N_b = 3 + 10\log_{10}(2) =$ 6 dB for 4-QAM/QPSK modulation at BER $= 10^{-1.5}$ (see Figure E.1), and thus, a raw data rate of only $4 \times 1.76 \times \log_2(4) = 14.04$ Gbps is achievable, using the proposed HSSW-I with four-channel bonding. Notice that the BER for this case is higher. Hence, it is important to note that the concurrent communication between many antenna pairs will be limited in data rate and error-prone, especially if the pairs are close to one another. One option is to have only one antenna pair communicate at a time, which will minimize the interference generated and allow higher data rates at lower BER. For larger MAM modules containing higher number of antenna pairs, simultaneous high throughput communications involving distant antenna pairs are

possible as the interference power is suppressed due to larger separation between the communicating and interfering pairs. The network layer NoC protocol could be designed based on the in-situ BER to dynamically determine the antenna pairs which are allowed to communicate simultaneously, and thus, optimize the network traffic and increase the computational speed.

4.7 Comparison With Four-Element Star Array

In this section, the transmission coefficient $|S_{CE}|$ of the antenna module pair is compared with that of the antenna array found in [42]. The four-element star array of [42] is a switched-element antenna and requires the use of a larger switch network instead of a feed network. The four antenna elements are switched individually or in pairs to scan the main beam along the four diagonal directions. A TX/RX pair of the star array separated by $R = 20$ mm, is modeled in HFSS for the Case 1 given in [42], as shown in Figure 4.11. The elements of the pair are excited to have the main beams of the antennas pointed at one another. The switch network and its associated losses are not considered in the simulation.

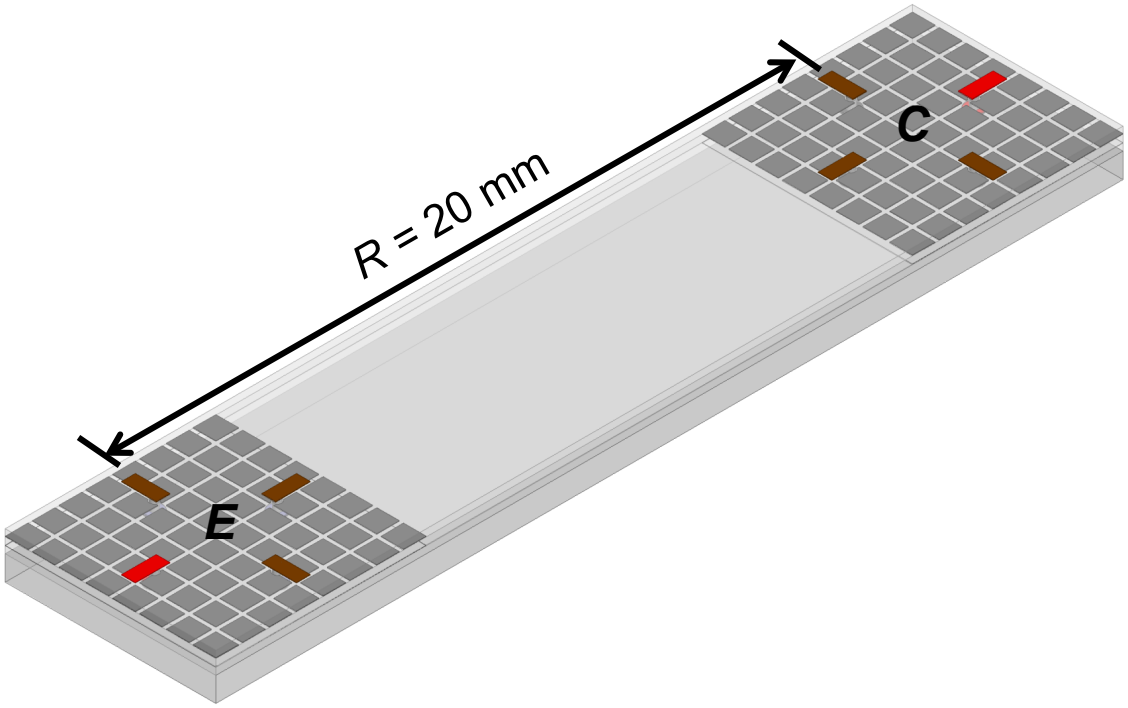


Figure 4.11. 3-D model of the pair of four-element star arrays of [42], separated by $R = 20$ mm. The switch network is not modeled.

The transmission coefficient $|S_{CE}|$ of the antenna module developed (i.e., with feed network) and the star array are shown in Figure 4.12. The antenna module has a relatively flatter transmission with gradual changes whereas the star array has abrupt changes in transmission. A flat transmission will relax the design requirement of the LNA and eventually reduce BER in QAM schemes [25]. The star array, on average, has a higher transmission but this is mostly due to a thicker substrate and unaccounted losses in the switch network, both of which must be considered for a better comparison.

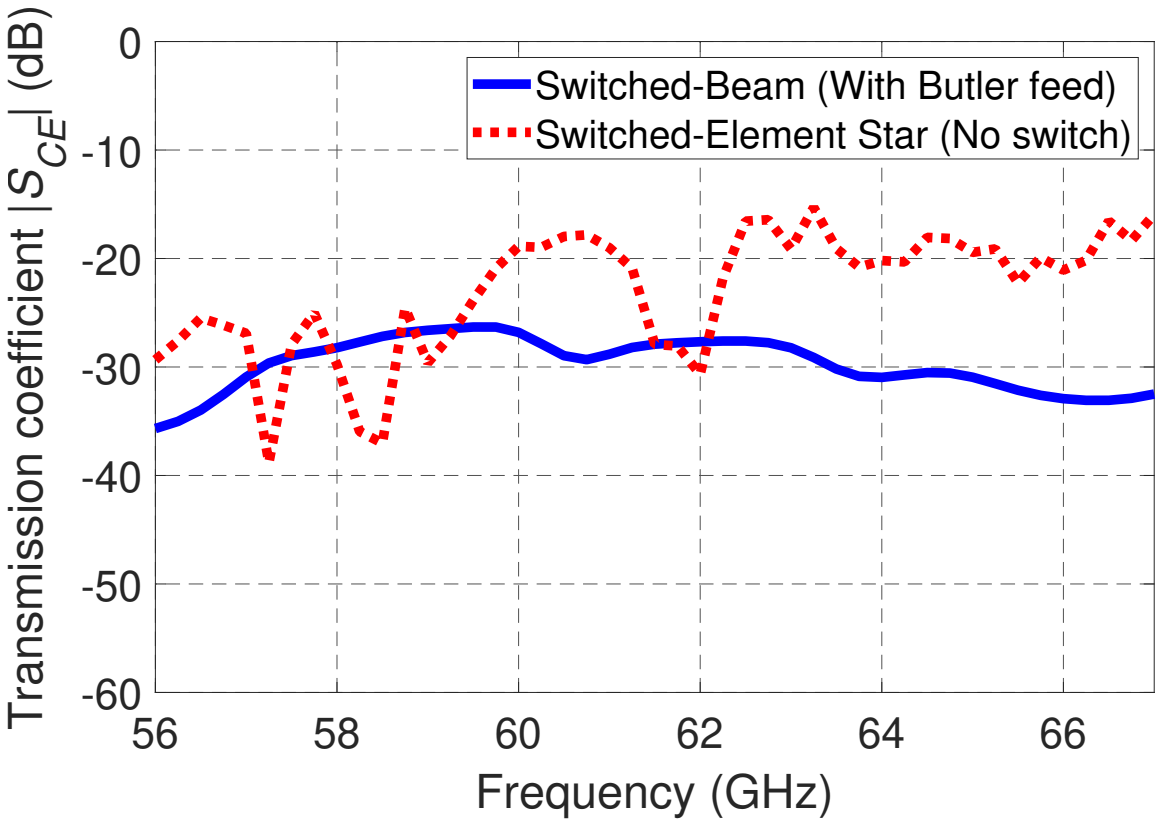


Figure 4.12. Comparison of the simulated transmission coefficients $|S_{CE}|$ of the antenna module and the four-element star array.

4.8 Link Model With Leaky Wave Effects

In this section, the horizontal transmission $|S_{CE}|$ between the antenna modules E and C on the MAM is modeled based on the presence of significant leaky wave effects. The grounded substrate of the HSSW-I allows surface waves to propagate but a leakage mechanism is observed. The circular patches form a leaky parallel-plate waveguide structure with the ground plane. The patch array behaves as a finite 2-D periodic leaky wave antenna. The Brillouin diagram for the structure shows that the first order negative Floquet harmonic of the fundamental parallel-plate mode is responsible for the leakage. A transmission model is devised based on these observations. The leakage coefficients are solved using simulation data to provide accurate estimation

of broadband link power at various distances.

4.8.1 Introduction

The power coupling between two circular patch antennas on a grounded dielectric substrate along the air-dielectric interface has been shown to consist primarily of lateral and surface wave components at large distances [60, 61]. At a far enough distance R from the patch antenna, the lateral wave power decays as $1/R^4$ and the surface wave power decays as $1/R$ along the interface [60]. The surface waves improve signal transmission especially at large distances because they decay slower compared to the lateral waves. Therefore, for horizontal communications, the HSSW-I has higher power coupling than the traditional wireless link. The horizontal transmission $|S_{CE}|$ between the antenna array modules is modeled from 56 to 67 GHz.

The nature of the power coupling between the patch arrays shows significant leaky wave decay behavior. This has not been observed for the TX/RX pair of single patch antennas, neither for conventional [82] nor for shorted [60]. The periodic nature of the array is shown to be the cause for the leaky wave effect. The 2 $\times$ 2 circular patch array is 2-D periodic, with the periodicity being the interelement separation. Physically, the patch arrays act as a partially reflective surface of the parallel-plate waveguide formed between them and the ground plane. The fundamental parallel-plate mode is perturbed, and leakage occurs [90–92]. The Brillouin diagram for the structure, considering the periodicity of the circular patches in the array, shows that the first order negative Floquet harmonic of the fundamental parallel-plate mode is in the fast wave region (FWR) for the frequencies considered. The harmonic leaks into both the space and surface waves at broadside [90] and thus exponentially reduces the horizontal transmission with distance. This leaky wave effect is taken into account in the transmission modeling equation. The frequency-dependent attenuation/leakage coefficients are determined from the simulated transmission data. The measured and

simulated $|S_{CE}|$ are compared with the results obtained from the link model. The transmission model is then extrapolated at different distances and compared with more measurement and simulation results.

The modeling of link associated with the communicating pair i.e., E–C in Figure 4.1 is considered due to its higher transmission levels and symmetric beam configuration. The link modeling associated with the interfering pairs are challenging due to low transmission levels and asymmetric beam configuration and it will be the subject of future works. Therefore, the link model only applies to the antenna pairs when their main beams are pointed at one another.

4.8.2 Leaky Wave Effect and Brillouin Diagram

The electric field of a traveling-wave structure with periodic loading in both x- and y-directions (e.g., in Figure 4.13 but with infinite periodic array), in terms of spatial harmonics of its fundamental mode [93], in cylindrical coordinates, can be expressed as

$$\vec{E}(\rho,\phi,z) = \sum_{m,n=-\infty}^{\infty} \vec{a}_{m,n}(\phi,z)e^{-j\vec{k}_{\rho mn}\cdot\vec{\rho}} \tag{4.19}$$

where $\vec{a}_{m,n}(\phi,z)$ is the transverse electric field of (m,n) spatial harmonic. The propagation phase is

$$\vec{k}_{\rho mn}\cdot\vec{\rho} = k_{xm}\rho\cos\phi + k_{yn}\rho\sin\phi \tag{4.20}$$

where

$$k_{xm} = \beta_{x0} + \frac{2\pi m}{d} - j\alpha_x \qquad m = 0,\pm1,\pm2,... \tag{4.21a}$$

$$k_{yn} = \beta_{y0} + \frac{2\pi n}{d} - j\alpha_y \qquad n = 0,\pm1,\pm2,... \tag{4.21b}$$

For propagation along the $\phi = 45^\circ$ diagonal direction, and knowing $\beta_{x0} = \beta_{\rho0}\cos\phi$ and $\beta_{y0} = \beta_{\rho0}\sin\phi$, (4.20) after substituting (4.21), simplifies to,

$$\vec{k}_{\rho mn}\cdot\vec{\rho} = (\beta_{\rho mn} - j\alpha_\rho)\rho \tag{4.22}$$

with

$$\beta_{\rho mn} = \beta_{\rho 0} + \frac{2\pi(m+n)}{d_\rho} \tag{4.23}$$

where $\beta_{\rho 0}$ is the phase coefficient and α_ρ is the attenuation coefficient of the fundamental parallel-plate mode, $\beta_{\rho 0}$ is the (m, n) Floquet harmonic, and $d_\rho = d\sqrt{2}$ is the periodicity along the radial propagation direction. α_ρ is associated with the loss along the radial direction due to the leakage. α_ρ also includes conductor and dielectric losses α_{cd} if they are present.

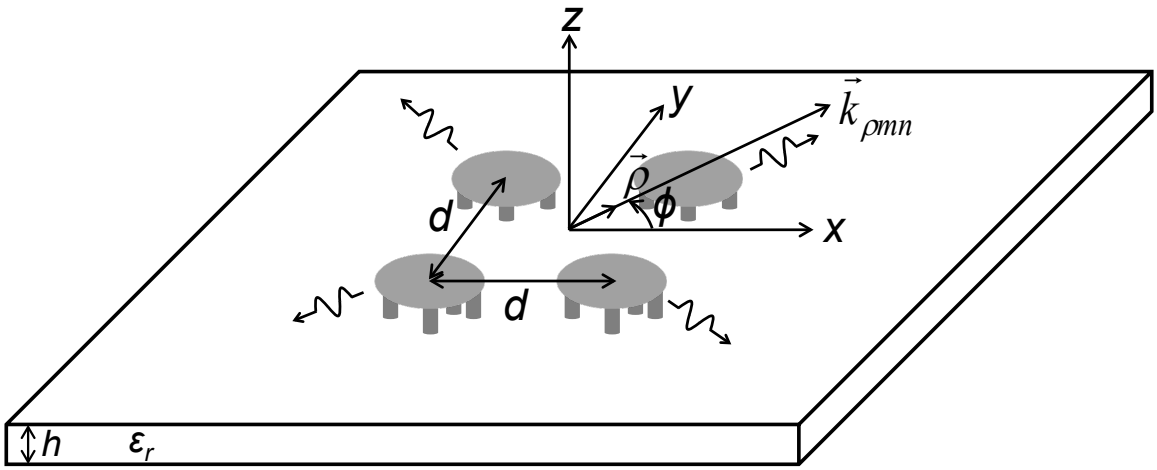


Figure 4.13. 2-D periodic leaky wave patch array on a grounded dielectric substrate.

The center-fed shorted circular patches in Figure 4.13 act as parallel-plate radial waveguides since $h \ll \lambda_0$ where λ_0 is the free-space wavelength at 60 GHz. The feed current flows along the z-direction on the center feed and side vias, which excites the TM^z modes. The propagation wavenumber of TM^z modes in a parallel-plate radial waveguide [84] is given by

$$\beta_{\rho q} = \sqrt{\beta_{\rho 0}^2 - \left(\frac{q\pi}{h}\right)^2} \qquad q = 0, 1, 2, ... \tag{4.24}$$

The $q = 0$ mode has zero cutoff frequency and is the fundamental mode with $\beta_{TM_0} < \beta_{\rho 0} < \beta_d$, depending on the type and degree of periodic loading [94], where $\beta_d = k_0\sqrt{\epsilon_r} = k_1$ is the dielectric wavenumber, k_0 is the free-space wavenumber

and β_{TM_0} is the TM_0 surface wavenumber of the grounded substrate. The circularly (ϕ) symmetric nature of the patches and the vias excites the $q = 0$ mode (which is also symmetric in ϕ). The $q > 0$ modes are cut off for the given h and frequency range considered. For vanishingly small loading, $\beta_{\rho 0} \to \beta_{TM_0}$ and for infinite periodic loading, $\beta_{\rho 0} \to \beta_d$. The Brillouin diagram, shown in Figure 4.14, is a plot of $k_0 d_\rho/\pi$ versus $\beta_\rho d_\rho/\pi$. Despite the lack of quantitative knowledge of $\beta_{\rho 0}$, the leaky wave effect can be analyzed since the bounds are known. The range of possible values of $\beta_{\rho 0}$ is indicated by $(m+n) = 0$ (fundamental mode) angular region (i.e., angle ψ) in Figure 4.14. This angular region also manifests in the $(m+n) = -1$ harmonic.

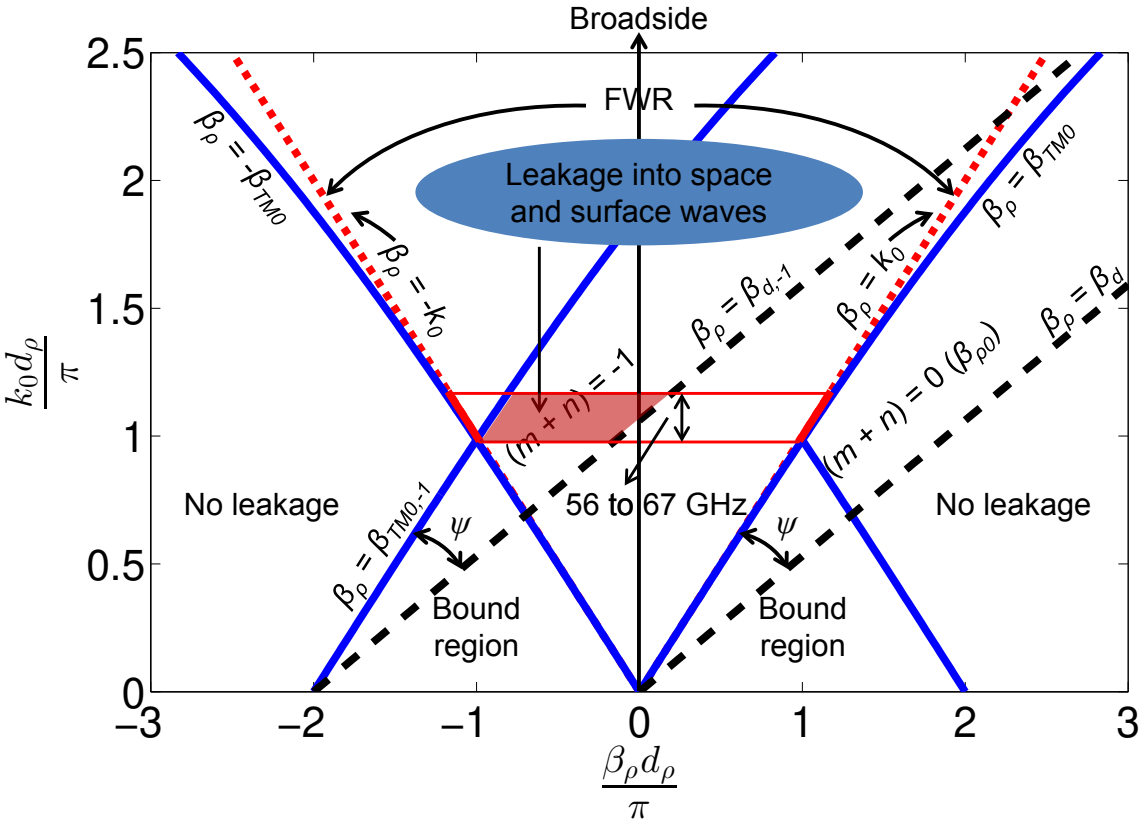


Figure 4.14. Brillouin diagram showing the $(m+n) = -1$ Floquet harmonic of the fundamental parallel-plate mode $\beta_{\rho 0}$. The harmonic is in the FWR for the given frequency range and leaks into free-space and TM_0 surface wave.

The waves with fast wavenumbers can phase-match with k_0 and β_{TM_0}, within some

range of elevation angle θ and leak. Since $\beta_{\rho 0} > \beta_{TM_0} > k_0$, the fundamental mode i.e., $(m+n) = 0$ in (4.23), is a slow, non-radiating wave and does not leak significantly. The (m, n) Floquet harmonic, however, can be fast i.e., $-k_0 < \beta_{\rho mn} < k_0$, for certain order $(m+n) < 0$ in (4.23). Specifically, the first order negative harmonic, i.e., $(m+n) = -1$ is well within the FWR of the diagram from 56 to 67 GHz (indicated by the shaded strip, which overlaps with the angular region ψ of the harmonic). The harmonic includes $(m, n) = (0, -1), (m, n) = (-1, 0), (m, n) = (1, -2), (m, n) = (-2, 1)$, and so on. They have positive group velocities as indicated by the positive slope of the boundaries of $(m+n) = -1$ angular region in Figure 4.14, which is consistent with the radially outgoing power flow. The lower order m and n harmonics will dominate the leakage since the convergence of (4.19) requires $|\vec{a}_{m,n}|$ to decrease as $|m|, |n| \to \infty$ [94]. Therefore, the first order harmonics $(-1, 0)$ and $(0, -1)$ will be primarily responsible for the leakage. The harmonics leak around the broadside direction, into both the free-space as well as the TM_0 surface wave of the grounded dielectric substrate [90] and reduce horizontal transmission. The $(m + n) = -1$ harmonic with negative slope/group velocities (not shown) would also lie in the FWR but it does not have to be considered because of radially outgoing source excitation [94]. Furthermore, there is no leak into the TE_1 and higher order modes of the substrate since they are cut off. The $\beta_\rho = \pm\beta_{TM_0}$ curves in Figure 4.14 are obtained by finding the root of the TM^z characteristic equation of the grounded substrate [84], which takes the following form after substituting (3.15) and (3.16) in (3.14):

$$\epsilon_r \sqrt{\beta_{TM_0}^2 - k_0^2} = \sqrt{\beta_d^2 - \beta_{TM_0}^2} \tan\left(\sqrt{\beta_d^2 - \beta_{TM_0}^2} h\right) \tag{4.25}$$

4.8.3 Link Modeling Equation

From (4.19) and (4.22), it is clear that the leaky waves cause the electric field to decay exponentially with distance R along the air-dielectric interface. The leakage away from the interface is modeled using exponentially decaying lateral and TM_0

surface wave terms in the horizontal transmission equation as follows:

$$|S_{CE}(f,R)|^2 = |S^l_{CE}(f,R)|^2 + |S^s_{CE}(f,R)|^2 \tag{4.26a}$$

$$= \frac{A_l(f)e^{-2\alpha_{\rho l}(f)R}}{R^4} + \frac{A_s(f)e^{-2\alpha_{\rho s}(f)R}}{R} \tag{4.26b}$$

where $|S_{CE}(f,R)|$ represents the frequency- and distance-dependent total transmission coefficient between antenna modules E and C in the horizontal plane, $|S^l_{CE}(f,R)|$ and $|S^s_{CE}(f,R)|$ are the lateral and surface wave components, respectively, $\alpha_{\rho l}(f)$ and $\alpha_{\rho s}(f)$ are the attenuation coefficients associated with leakage into free-space and surface wave (with $\alpha_{cd}(f)$ included), respectively, and $A_l(f)$ and $A_s(f)$ are the power coefficients corresponding to lateral and TM_0 surface waves, respectively. The link model indicates that the grounded dielectric substrate has both spreading and guided mode losses.

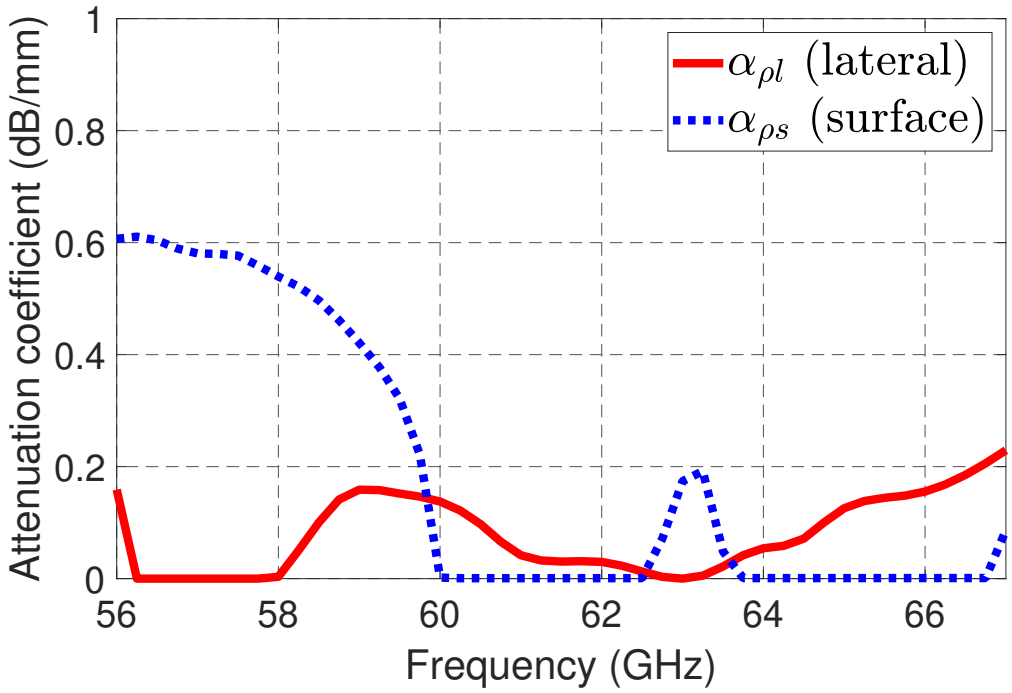
4.8.4 Link Model Coefficients

The link model should be able to provide an accurate estimate of power coupling between the modules E and C at various distances R without running exhaustive sets of full-wave simulations. In order to create an accurate broadband link model, the attenuation coefficients $\alpha_{\rho l}(f)$ and $\alpha_{\rho s}(f)$ are determined from two full-wave simulation data, one with $R = R_1 = 25$ mm and another with $R = R_2 = 27.5$ mm. These relatively larger distances are chosen to reduce the error in estimation caused by near-field perturbations in the simulated transmissions. Thus, four broadband simulations are required, two without and two with the in-between substrate and ground plane. Then, from (4.26b),

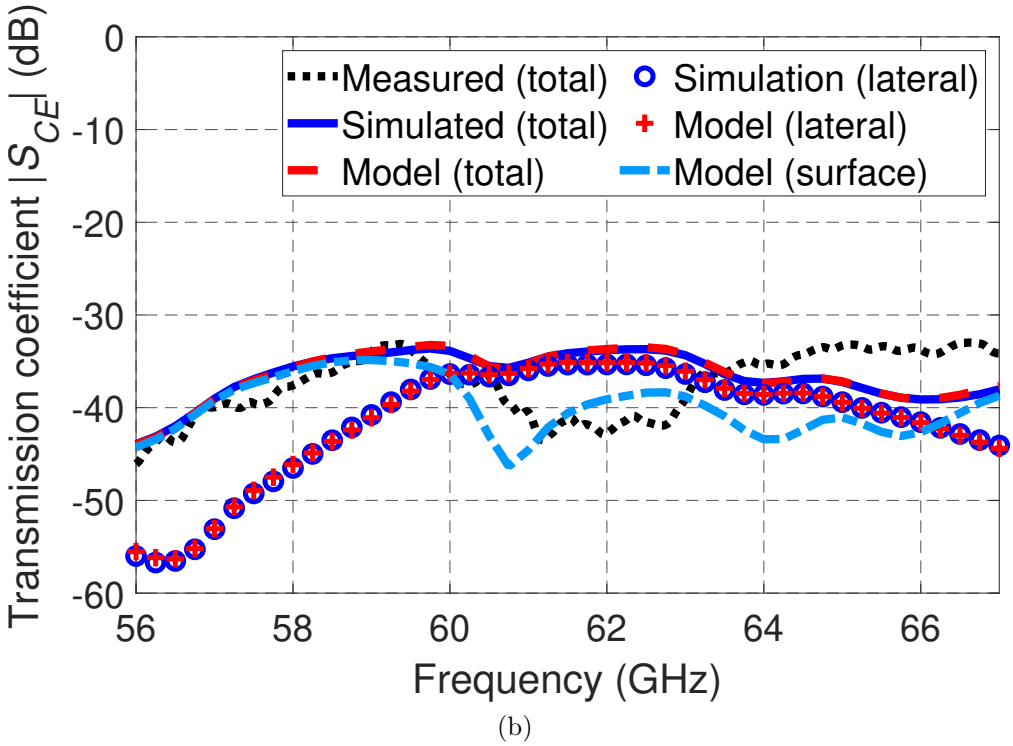
$$\alpha_{\rho l} = \frac{|S^l_{CE}(R_1)|_{\mathrm{dB}} - |S^l_{CE}(R_2)|_{\mathrm{dB}} - 40\log_{10}(R_2/R_1)}{8.686(R_2 - R_1)} \tag{4.27a}$$

$$\alpha_{\rho s} = \frac{|S^s_{CE}(R_1)|_{\mathrm{dB}} - |S^s_{CE}(R_2)|_{\mathrm{dB}} - 10\log_{10}(R_2/R_1)}{8.686(R_2 - R_1)} \tag{4.27b}$$

with the constraints $R_2 > R_1$, $\alpha_{\rho l} \geq 0$ and $\alpha_{\rho s} \geq \alpha_{cd}$, where $\alpha_{cd} = \mathrm{Im}[\beta_{TM_0}]$ is determined by using the complex dielectric constant ϵ_r' from (2.23) in (4.25). The calculated values are shown in Figure 4.15(a). The power coefficients $A_l(f)$ and $A_s(f)$ are then simply determined by normalizing the two terms in (4.26b) to the simulated $|S_{CE}^l(f, R_2)|^2$ and $|S_{CE}^s(f, R_2)|^2$ respectively. With the coefficients now determined, the model in (4.26b) is extrapolated at $R = 30.8$ mm and compared with the corresponding simulated and measured transmission. Another PCB prototype with $R = 30.8$ mm is fabricated in order to make the measurement. The results are shown in Figure 4.15(b). The total, lateral and surface wave components of the link model are plotted using (4.26).



(a)



(b)

Figure 4.15. (a) The attenuation coefficients $\alpha_{\rho l}(f)$ and $\alpha_{\rho s}(f)$ due to the leakage of the $(m+n) = -1$ Floquet harmonic. (b) Measured, simulated, and model transmission coefficients (dB) of the MAM with $R = 30.8$ mm.

The model is also extrapolated at $R = 20$ mm, as shown in Figure 4.16. There are good agreements, especially between the model and simulated results.

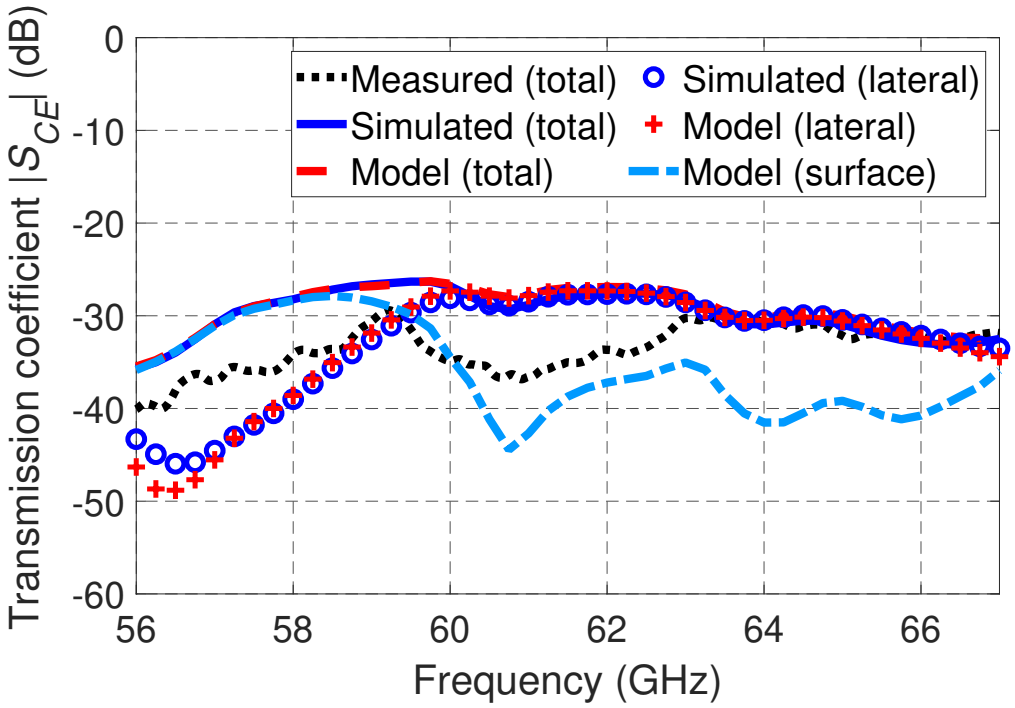


Figure 4.16. Measured, simulated, and model transmission coefficients (dB) with $R = 20$ mm.

Chapter 5
Manufacturing Deviation Considerations

A modified version of the Section 5.1 of this chapter has been published in [14]. Section 5.2 is scheduled to be published in [95].

5.1 Sensitivity to Via Diameters and Location, Dielectric Constant, and Losses

Previously in Section 2.4.4, it was shown that the array performance is most sensitive to variations in via diameter and location. Therefore, a sensitivity analysis simulation of the MAM with respect to the antenna parameters a_f, a_s and b is performed in order to consider possible manufacturing deviations [13] and their effect on the MAM performance. Small deviations in dielectric constants of the core and the prepreg, and higher loss tangents and conductor losses are also considered in the simulation. The increased conductor losses due to surface roughness is incorporated by using a lower effective conductivity (σ_{eff}) for the copper [67]. The analysis showed that when $a_f = a_s = 0.17$ mm and $b = 0.64$ mm with smaller dielectric constants and higher losses, the simulated reflection and transmission coefficients fair better with the measurement, as shown in Figure 5.1. There is a good agreement particularly between the simulated and measured $|S_{CE}|$, as shown in Figure 5.1(b). These parameter deviations are well within them manufacturing tolerances provided by the PCB vendor. The deviated values of the parameters used in the simulation are listed in Table 5.1 alongside their original values.

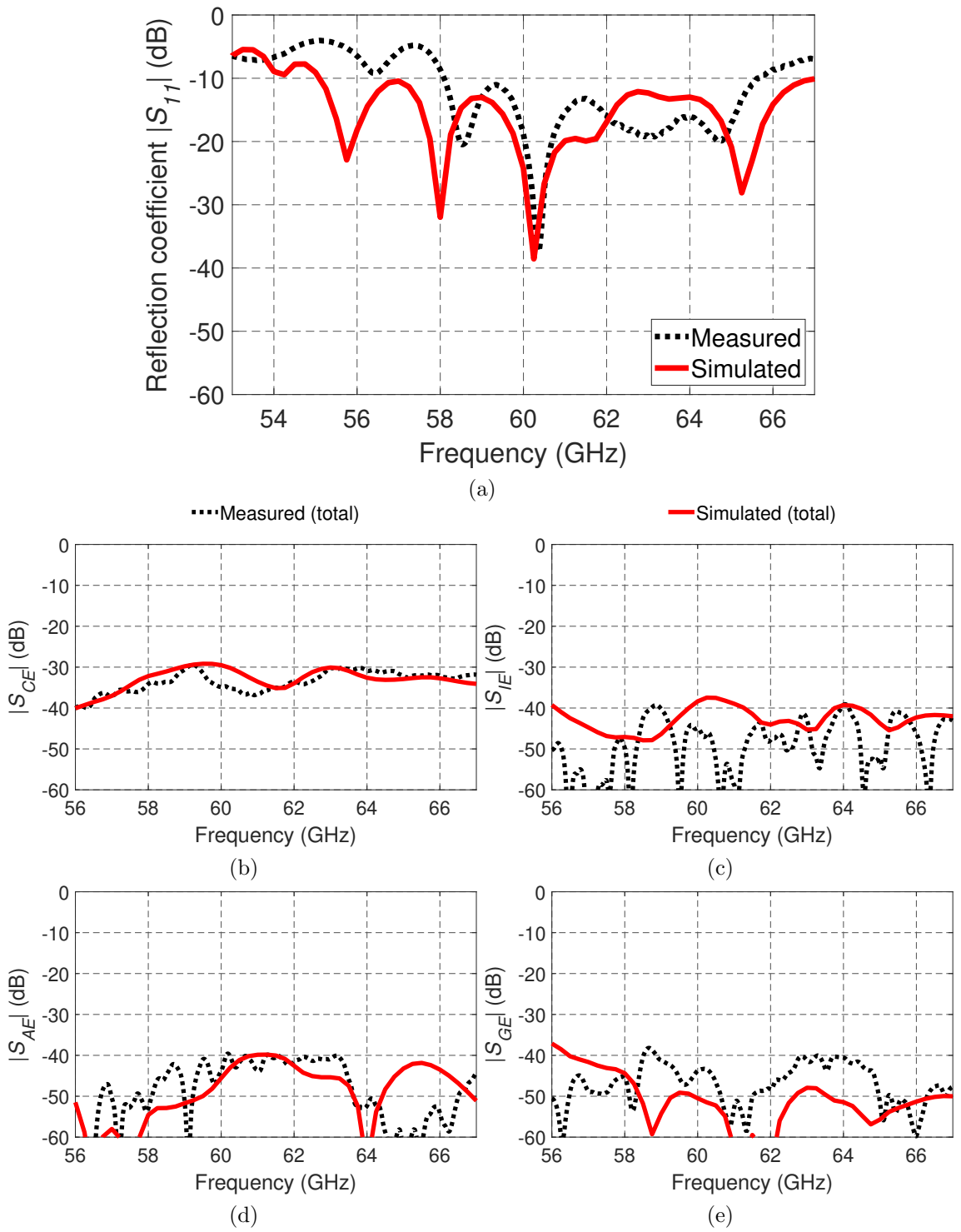


Figure 5.1. Comparison of the measurement with simulated S-parameters (dB) of the antenna modules on the MAM accounting for manufacturing deviations. (a) $|S_{11}|$. (b) $|S_{CE}|$. (c) $|S_{IE}|$. (d) $|S_{AE}|$. (e) $|S_{GE}|$.

Table 5.1. MAM parameter values with manufacturing deviations

MAM Parameter	**Original Value**	**Deviated Value**
Via diameters $a_f = a_s$	0.15 mm	0.17 mm
Via radial distance b	0.67 mm	0.64 mm
Core dielectric constant ϵ_r	3.55	3.5
Core loss tangent ($\tan\delta$)	0.0027	0.0035
Prepreg dielectric constant $\epsilon_{r,p}$	3.52	3.47
Prepreg loss tangent ($\tan\delta_p$)	0.004	0.005
Effective copper conductivity σ_{eff}	5.8×10^7 S/m	2×10^7 S/m

5.2 PCB Bowing Effects

In this section, the PCB bowing effects that are seen on the fabricated antenna modules are taken into account in the post-fabrication simulation. Only the bowing of an isolated antenna module [see Figure 3.11(b)] is considered whereas that of the MAM will need to be addressed in the future work. Thin multilayer PCBs are especially prone to bowing, which can be due to combination of factors such as asymmetrical stackup, uneven copper distribution, and mismatch in thermal expansion coefficients of the layers [96]. The bowing of multilayer PCBs can cause its electrical performance to deviate from design expectations. The curvature is introduced on the flat 3-D model of Figure 3.11(b) by intersecting the raised metal patterns with curve solid layers. The method is general and can be applied on any layered structure even if vias are present. The full-wave simulations of the model, with and without the bow, are performed. The deviations due to bowing in the reflection coefficient and radiation pattern of the antenna module are presented. The simulated reflection coefficients are also compared with the measurement to analyze whether bowing can account for the deviation, which is seen in the measurement.

5.2.1 Bowing Equations

The curvature of the board (e.g., its metal and dielectric layers) can be quantified by measuring the bow height b_h [97], as shown in Figure 5.2. The fabricated PCB module shows noticeable bowing only along one direction i.e., its width, and therefore, the bowing along the length is ignored. Although bowing in both directions can be incorporated by simple extension of the method presented.

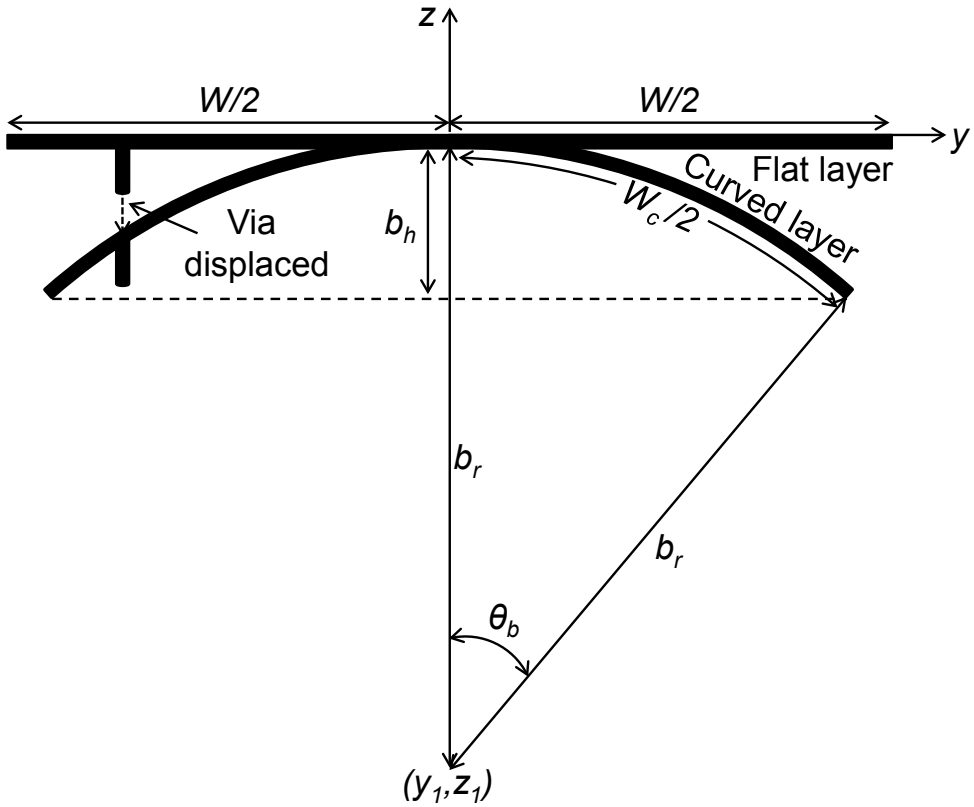


Figure 5.2. The bowing curvature of the metal/dielectric layers represented as the arc of the circle [95].

For modeling purposes, it is convenient to find the radius associated with the curvature, called the bow radius b_r. Given b_h and the board width W, the arc in the yz-plane with the center at $(y_1, z_1) = (0, -b_r)$, as shown in Figure 5.2, has the

following equation:

$$(y - y_1)^2 + (z - z_1)^2 = {b_r}^2 \tag{5.1}$$

where $-\frac{W}{2} \leq y \leq \frac{W}{2}$ and $0 \leq z \leq b_h$.

From (5.1), the points (y, z) on the arc are related by

$$z = -b_r + \sqrt{{b_r}^2 - y^2} \tag{5.2}$$

In Figure 5.2, for small b_h, the length of the arc $W_c \rightarrow W$. Thus, the bow angle θ_b is given by

$$\theta_b = \frac{W_c}{2b_r} \approx \frac{W}{2b_r} \tag{5.3}$$

Also,

$$\cos\theta_b = \frac{b_r - b_h}{b_r} \tag{5.4}$$

From (5.3) and (5.4),

$$\cos\frac{W}{2b_r} = \frac{b_r - b_h}{b_r} \tag{5.5}$$

Equation (5.5) can be solved numerically for b_r. Once b_r is found, the metal and dielectric layers of the structure can be curved in HFSS [98].

5.2.2 Bowing of 3-D Model

The flat and curved 3-D models of the multilayer antenna module are shown in Figure 5.3. The curved model is created from the flat model using the following sequence of steps:

1. The curved solid layer with radius b_r is generated for each metal and dielectric layer at their corresponding z-coordinate. To accomplish this, the top and bottom curved surfaces of each layer are created separately using equation-based curves in HFSS, and then joined to form the curved solid layer (see Figure 5.4).

2. The metal layer patterns are imprinted on their corresponding curved layer. The existing flat metal patterns are first raised so that they overlap with the

curved solid layer, followed by a Boolean intersection of the two. This step is illustrated for the feed layer in Figure 5.4.

3. The ports, and the vias, if present, are displaced by distance z (along the z-direction), as given by (5.2), depending on their y-distance from the origin (see Figure 5.2).

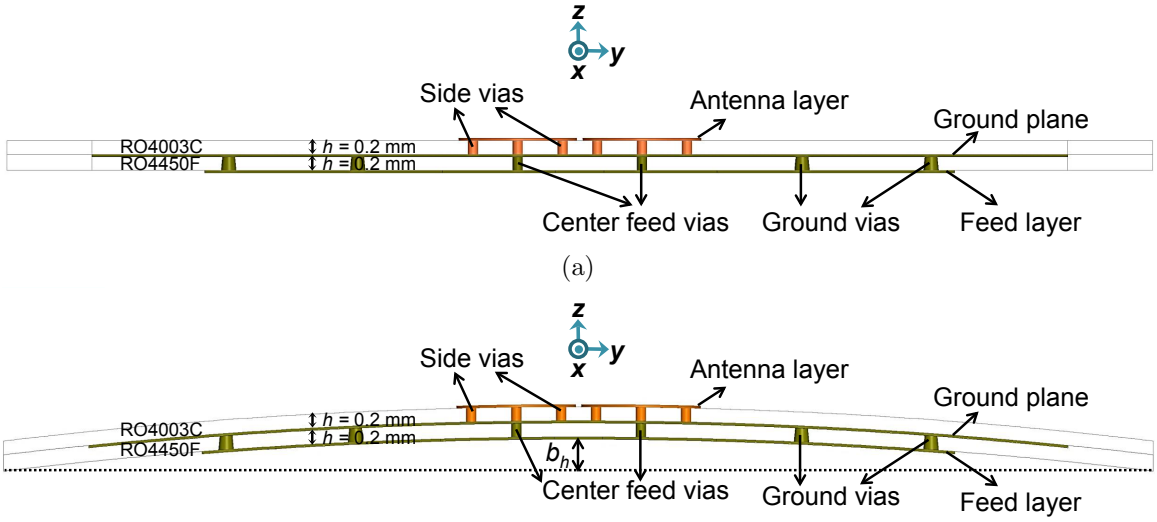


Figure 5.3. Side view of the multilayer antenna module [95]. (a) Flat 3-D model. (b) Curved 3-D model.

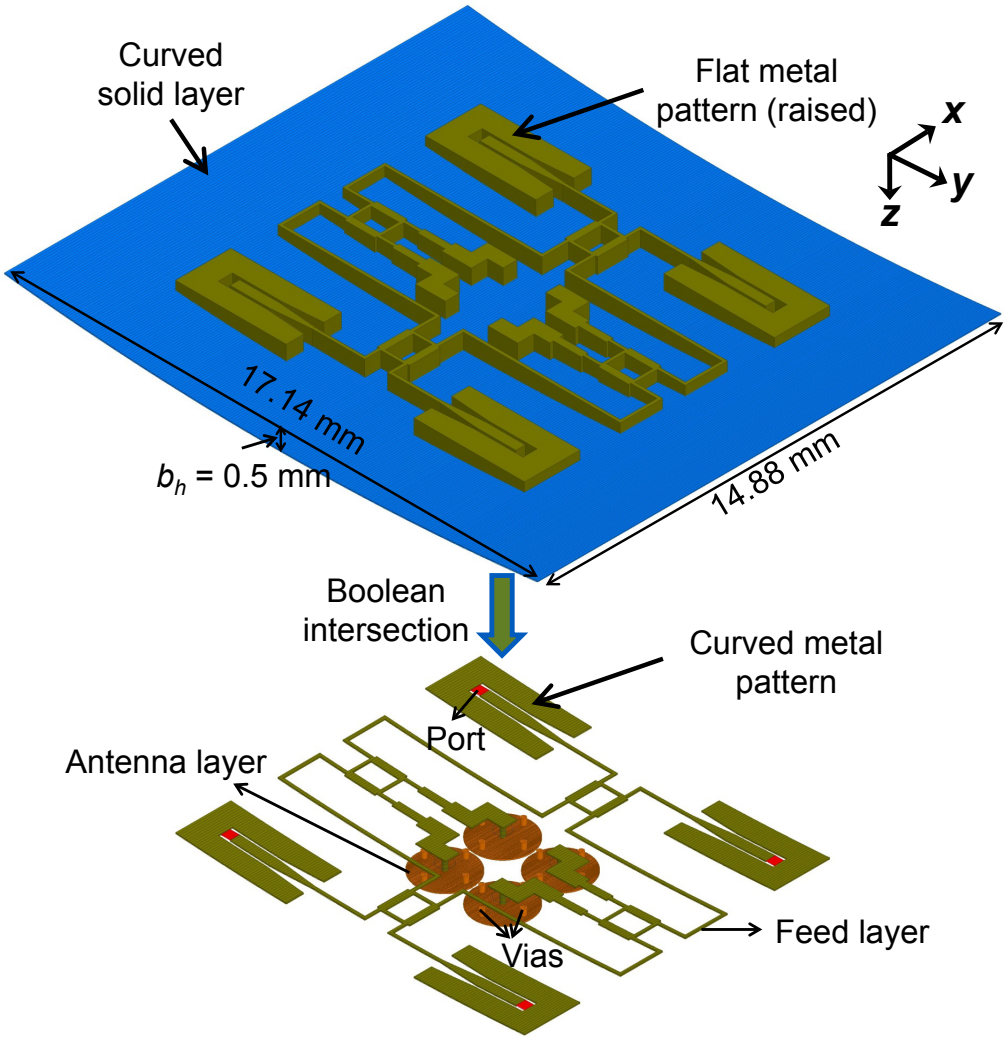


Figure 5.4. The flat metal patterns in the feed layer are curved by first raising the flat metal patterns (green) and then intersecting them with the curved solid layer (blue) [95].

5.2.3 Bowing Results and Comparison

The flat and curved 3-D models, as shown in Figure 5.3, are simulated in HFSS. Curvilinear tetrahedra are used during meshing for better accuracy and speed since they conform better with the curved geometry using fewer elements [98]. Figure 5.5 shows the measurement setup, measured and simulated reflection coefficients, and

the simulated 60 GHz horizontal gain patterns of the antenna module corresponding to $b_h = 0.5$ mm (3% *bow*, $b_r = 73.3$ mm) and *no bow* cases. As shown in Figure 5.5(b), bowing has slightly decreased the overall reflection coefficient levels. The measured curve has a slight frequency shift, attributed to the manufacturing and probe placement variations. The measured impedance BW of the isolated module is 8.25 GHz. The SLLs, as shown in Figure 5.5(c), have decreased in the angular region $-5^\circ < \phi < 45^\circ$ but increased in the angular region $180^\circ < \phi < 215^\circ$, due to bowing. The maximum SLL has lowered by 1 dB but there are no changes in the main beam shape and level.

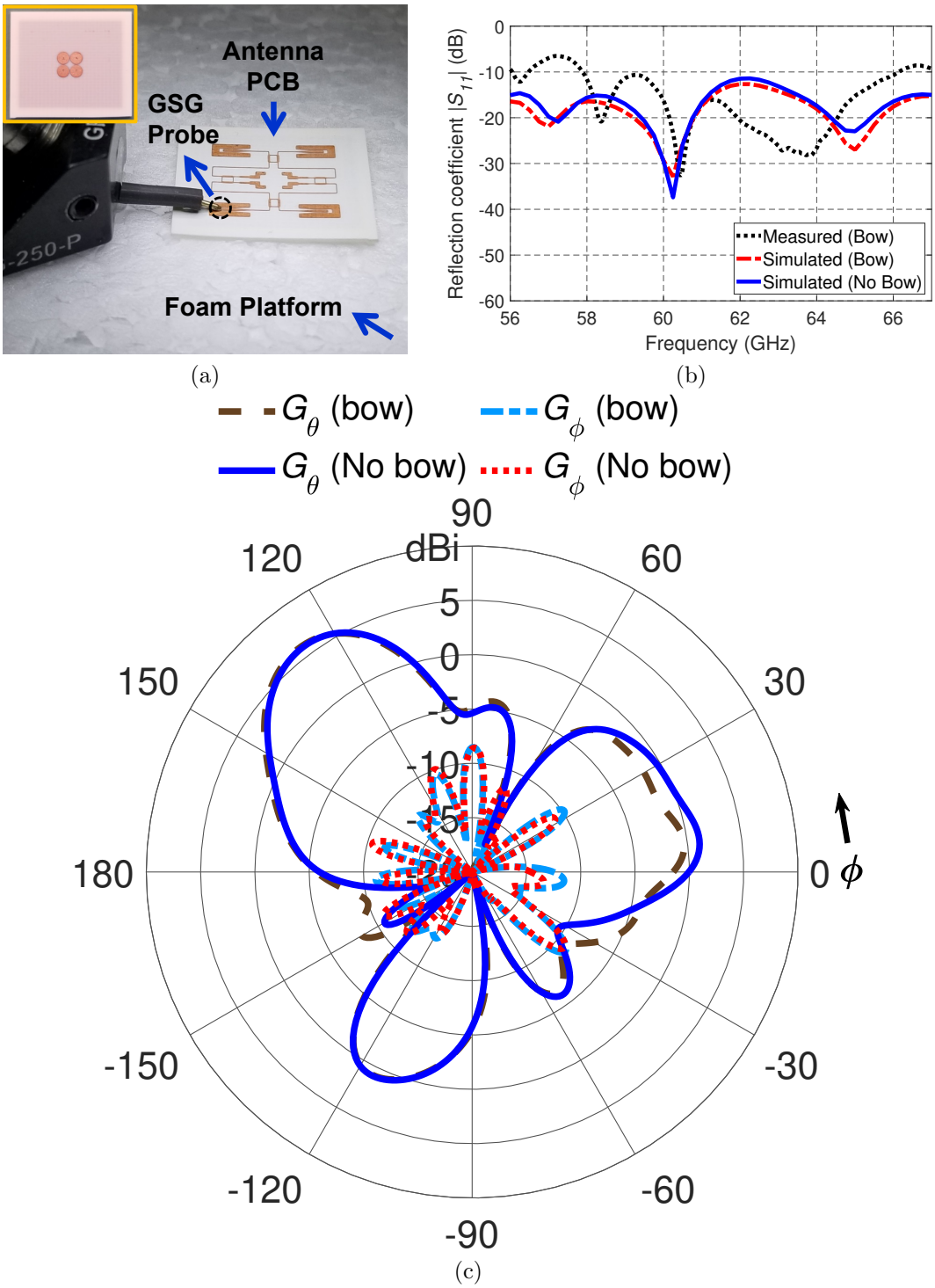


Figure 5.5. (a) Measurement setup of the fabricated PCB module [95]. (b) Reflection coefficients of the fabricated PCB [95]. (c) 60 GHz simulated gain patterns (dBi) in the horizontal plane ($\theta = 90°$) [95].

Chapter 6
Conclusion and Future Works

6.1 Conclusion

This dissertation presented and analyzed a new type of hybrid space-surface wave interconnect (HSSW-I) for reconfigurable and high throughput chip-to-chip communications in multicore multichip (MCMC) modules at 60 GHz. This section concludes all the major ideas and research findings discussed in each of the previous chapters of this dissertation.

In Chapter 1, the HSSW-I was introduced as an alternative to global wired interconnects in large computing systems such as the MCMC. It solves the wiring complexity and lengthy delays associated with long wires by using 60 GHz switched-beam antenna arrays. Furthermore, the HSSW-I combines the low design complexity of millimeter-wave (mmW) wireless interconnect with the lower path loss of surface wave interconnect (SW-I). The HSSW-I uses a low-loss interconnection substrate to take advantage of both space and surface wave coupling between the antennas and thus increases link transmission.

In Chapter 2, the 60 GHz circular patch planar arrays were designed and analyzed to generate four switchable diagonal endfire beams in the horizontal plane. These enabled chips packaged with the arrays to dynamically communicate to their four diagonal neighbors without using wires. The main beam of the array was switched by exciting the elements with proper phase shifts. Full-wave simulation of the array verified the switching of the main beam. The gain patterns of the array were analyzed which showed the endfire nature of the main beam. A sensitivity analysis was also conducted which indicated that the array performance was most sensitive to the deviations in the via diameters.

In Chapter 3, the 2-D Butler matrix in microstrip (MS) form was designed to

realize the interelement phase shifts required for the switched-beam array. The operation of the Butler matrix and its various components was verified with the full-wave simulation. The matrix was then integrated with the array by stacking the layers. The main beam of the integrated multilayer antenna module can be simply switched by individually exciting the different ports. The antenna module had a more directive main beam in the horizontal plane but lower gain bandwidth (BW) than the standalone array. The electric field distribution in the vertical plane showed the radiation and surface wave dominated regions of the module.

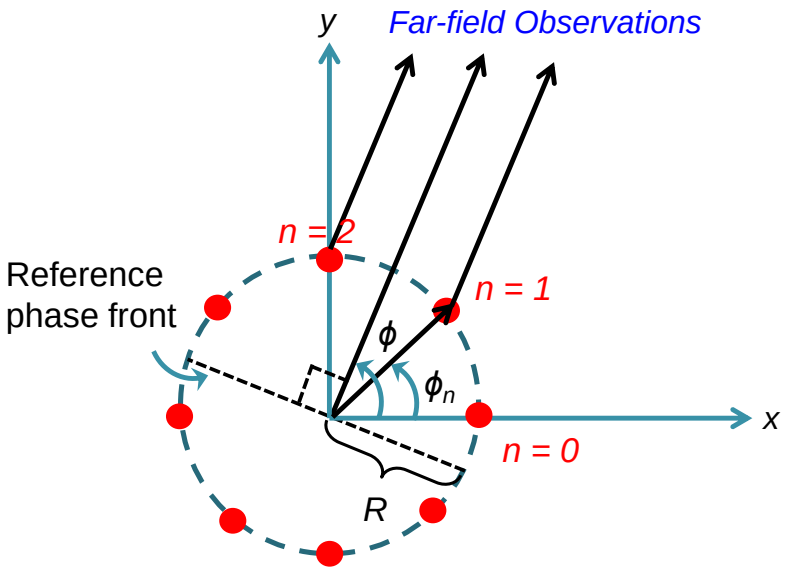
In Chapter 4, the HSSW-I was realized by putting together five antenna modules on a low-loss substrate with the common ground plane underneath. The multi-antenna module (MAM) was fabricated using printed circuit board (PCB) techniques. The reflection coefficients were measured and showed good agreement with the simulation. A measured impedance BW of 7.57 GHz was attained for an antenna module on the MAM. A pair of modules with their main beams pointed at one another were designated as the communicating pair while the others were designed as the interfering pairs. The transmission coefficients among the pairs were measured and simulated. The signal transmission BW was simulated to be 6.25 GHz. The transmission coefficient data were used to calculate the signal-to-noise ratio (SNR) which indicated that the HSSW-I is capable of achieving up to 42.24 Gbps data rate at 20 mm distance in the absence of interference. The calculated signal-to-noise-plus-interference ratio (SNIR) showed that data rates up to 14.04 Gbps is possible, although with higher bit errors, when interference from neighboring antenna modules were considered. A new link model specific to the antenna arrays was introduced and the link coefficients were determined from the simulated data. The link model was verified by extrapolation and comparison with measurement and more simulation data.

In Chapter 5, the effect of the possible manufacturing deviations on the performance of the HSSW-I and antenna modules were addressed. Full-wave simulation results showed that a combination of small deviations in via diameters and loca-

tion, substrate dielectric constant, and higher dielectric and conductor losses were the probable cause of the small difference between the measurement and simulation. The bowing seen on the fabricated prototypes were also modeled and simulated to determine its effects. The results for an individual antenna module with and without bowing were compared.

6.2 Future Works

To provide more coverage, the antenna module in the future work should consider beam scanning in all eight directions. This will allow a chip to communicate to all its eight neighbors further improving the reconfigurability of the HSSW-I. A full 360° angular coverage in small steps can be achieved by using a uniform circular array (UCA), as shown in Figure 6.1 with little to no variations in beam shape with scan angle. However, this requires a co-sinusoidal phase taper among the elements of the array. To achieve the taper, a Butler matrix can be used but requires proper linear to circular phasing transformations at the input of the matrix [99]. This can drastically increase losses as more components are required.

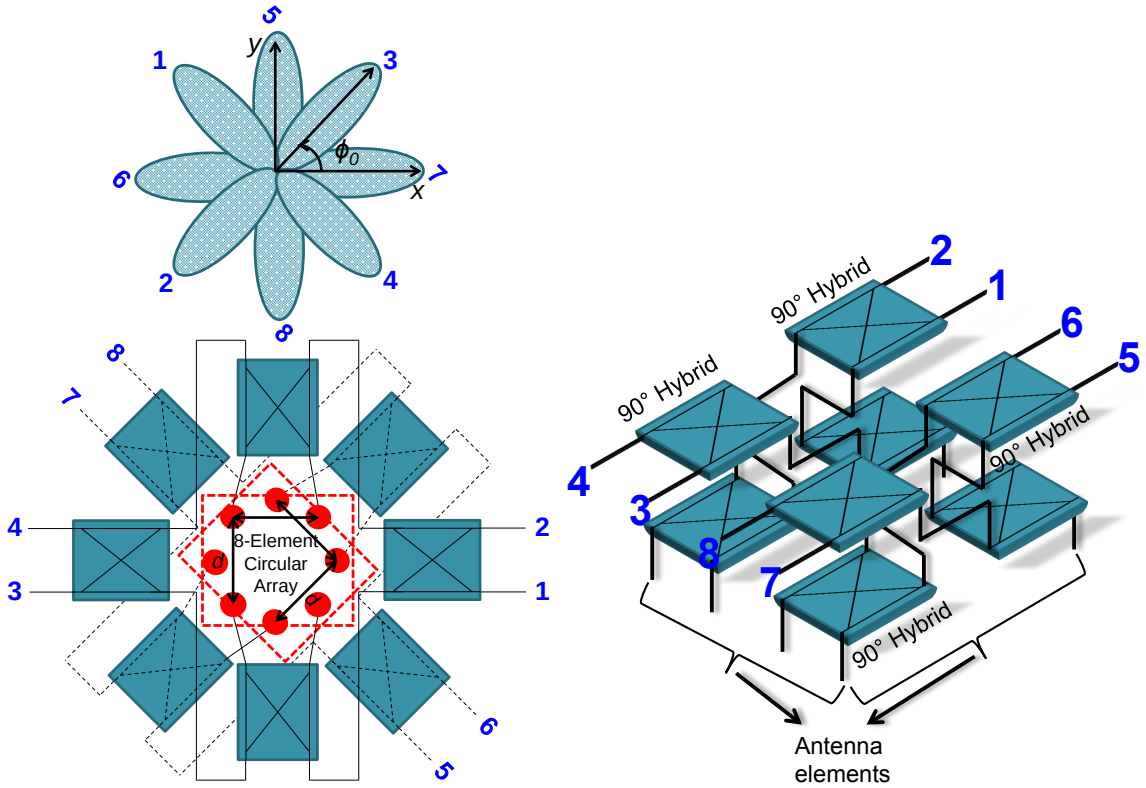


Main beam condition

$$\beta_e(n) = -k_0 R \cos(\phi - \phi_n)$$

Figure 6.1. UCA with eight elements for full angular coverage.

An alternative feeding method can be arrived at by thinking of the eight-element UCA as the combination of a 2 × 2 planar array with another 2 × 2 planar array that is rotated by 45°. Note that the elements should be small enough to avoid any overlap and therefore, they would have to be miniaturized. Each 2 × 2 array could be fed by the 2-D Butler matrix described in this dissertation, as illustrated in Figure 6.2(a). The link losses will increase because an additional SP2T switch will be required at the front to switch between the two SP4T switches. The two Butler matrices could be 3-D (vertically) stacked across two signal layers to avoid the overlap and also reduce the overall feed network footprint, as depicted in Figure 6.2(b).



(a) (b)

Figure 6.2. (a) An eight-element circular array fed with the two 2-D Butler matrices for eight beam scanning. (b) Stacked Butler matrices.

The unwanted coupling between the feed layer and chips underneath must also be minimized to reduce the background noise picked up by the antenna module. This could be done by implementing the feed network in stripline form which virtually shields the feed layer from outside interference. This also minimizes unexpected changes in antenna performance when the module is packaged with the chip.

Finally, the SLLs of the arrays should be minimized, e.g., through multiple null formation, in order to reduce unwanted radiation (interference) toward unintended receivers and improve the SNIR of the links. The feed network for the array should be designed to achieve simultaneous main beam and null formation to direct power only in the intended directions [100].

Appendix A
Interconnect Technology Types and Topology

A.1 Interconnect Technology

A.1.1 Three-Dimensional (3-D) Integrated Circuit (IC) Interconnect

3-D ICs are often implemented by vertically stacking multiple dies of 2-D ICs [1]. Through-silicon vias (TSVs) are etched through the dies to provide dense interconnection between the layers and hence a way to realize 3-D mesh topology [10]. The vertical interconnects can also offer shorter global connections with reduced hop count since there is an additional dimension for routing. However, higher interconnect density also results in higher power consumption density and thermal management becomes necessary. Use of thermal vias and microfluids for cooling increases the design complexity [101]. Manufacturing challenges such as precise wafer alignment and TSV induced mechanical stress still remain. Furthermore, although the shorter vertical interconnects provide lower delay, they are still based on conventional metal/dielectric system that will eventually reach a performance cap. Thus, they are not expected to keep up with transistor delay improvement offered by future process generations. One advantage of 3-D interconnects is that the signals can propagate at baseband frequencies and additional transceiver circuits are generally not required, just like in the conventional wired interconnects.

A.1.2 Optical Interconnect

Interconnects based on optical devices can potentially offer much higher BW and longer range with low attenuation at the speed of light [11]. However, such interconnects have not been easily and efficiently integrated with CMOS devices yet. Some optical devices are needed for electrical-to-optical (EO) and optical-to-electrical (OE)

conversions [102]. They have to be placed off-die resulting in high coupling losses. Silicon waveguide, silicon-based modulators and detectors have eliminated most of the integration issue, but an external laser source is still required due to the lack of efficient silicon laser. On-chip optical interconnects work well with tree topology and bus topology for global signal distribution. In tree topology, optical splitters are needed for distribution of signals, which would significantly reduce power after each branch point. This does not lend itself well to many-core systems, which benefits from efficiently interlinking the cores with minimum signal degradation. In bus topology implementation, wavelength division multiplexers (WDMs) are required to provide simultaneous access to a shared optical bus, increasing interconnect complexity. Optical interconnects are a costly alternative as a result of integration and manufacturing complexity.

A.1.3 Radio Frequency Interconnect (RF-I)

RF-Is offer on-chip waveguided propagation of signals at near the speed of light, generally meant for providing express links that are supplementary to the conventional wire [11]. Three major on-chip implementations of RF-Is are MS line (MSL), CPW, and coplanar strips (CPS). Integrated transceivers are required to convert low frequency electrical signal into high frequency RF signal and vice-versa, for transmission and reception, similar to the EO/OE conversions in optical interconnects. In some sense, RF-Is solve the integration problem associated with optical interconnects albeit at the cost of reduced BW. The RF-Is are limited in maximum operating frequency by the cut-off frequency of CMOS. In addition, the problem of signal distribution persists with RF-Is because of the inherent waveguiding nature. In tree topology implementation of RF-Is, signal power reduces in half, at each split point, that too if matching stubs are incorporated to prevent reflections. Bus topology implementation of RF-I requires frequency division multiplexing (FDM) to provide simultaneous mul-

tiple access to a shared RF-I bus [103]. Both implementations have manufacturing complexity with area overhead.

A.1.4 Millimeter-Wave (mmW) Wireless Interconnect

Wireless interconnects offer some of the most cost effective solutions with integrated transceivers and antennas compatible with CMOS technology [10,11]. The transceiver circuits can be fully integrated in CMOS with little area and power consumption overhead. Antenna radiation pattern could be configured to provide one-to-many communication (multicasting), at near the speed of light in the air above the chips. This can provide major performance improvement in many-core and multichip systems. Due to the inherent spherical spreading of antenna radiation, wireless interconnects can also offer single hop communication to multiple chips within their coverage area. This would greatly reduce latency associated with multi-hop communication, which is difficult to avoid in previously mentioned interconnect technologies. Challenges facing wireless interconnect are mainly on the antenna front. Highly efficient and wide BW on-chip antennas are hard to design, especially when the underlying silicon substrate is lossy and chip area is at a premium. However, as transistor feature size scales down, GHz and THz carrier frequencies with GHz BW are possible with smaller on-chip antennas [104]. Careful pattern configuration must be performed to focus the antenna beam and maximize transmission toward the intended receivers while simultaneously reducing interference to nearby circuits.

A.1.5 Surface Wave Interconnect (SW-I)

SW-I is an emerging technology that uses surface waves to guide the signal. Surface waves can propagate at the metal-dielectric interface at near the light speed [11]. Specially designed surfaces, such as the dielectric coated metal surfaces and corrugated metal surfaces, can be used to trap the surface waves at the 2-D interface with the

wave power decaying as $1/R$ along the boundary. This enables much better range than free-space wireless transmission in which the wave power decays as $1/R^2$. However, transducers must be embedded into the surface to launch and receive signals. Usually the transducer is a modified dipole or monopole antenna that must be connected to the integrated transceiver [105]. The surface with embedded transducer may be stacked on the CMOS circuits. This requires 3-D integration using TSV and flip-chip technology, which could increase manufacturing complexity. SW-Is are susceptible to interference from nearby circuits and interconnects. But SW-Is do generally offer better SNR, compared to wireless transmission, due to slower decay of signal with distance.

A.2 Interconnect Topologies

Interconnect topology refers to the way nodes (such as cores or chips) are physically interconnected and arranged in a NoC. The type of topology used has a major impact on network and overall system performance. Other factors affecting the choice of topology are chip area overhead, power consumption, hop count, latency, throughput, cost effectiveness, link redundancy, and ease of integration. Furthermore, differences in the interconnect technology characteristics can play a key role in topology selection. The topologies that are used in NoCs are bus, ring, mesh, and crossbar [10]. The most widely used are the bus and mesh topologies and they are briefly discussed here.

Bus topology utilizes a high speed shared medium (called the common bus) to which multiple cores are connected and that can only be used by one core at a time. Communication can be initiated by each core by driving the bus but simultaneous attempt to use the bus causes bus contention and wasted power. A bus arbiter module that controls access to the bus, is required to avoid contention. Bus arbitration can take multiple clock cycle, as a result of which the bus runs slower than the cores. Buses can become a critical performance bottleneck due to increased latency associated

with frequent bus arbitration in many-core systems [8]. Therefore, on-chip buses are usually used to connect only two to five cores. Although the shared bus provides a natural way for a core to broadcast the data, it comes with a power overhead. The bus must be driven with high power so that data can be received by all receivers. Due to performance bottleneck and power overhead, bus topology is not scalable to many-core systems [11].

In conventional mesh topology, each core is connected to its four adjacent neighbors [19, 104]. Communication between adjacent cores is fast but between distant cores across the chip can get increasingly slower because of more hops required. Mesh topology has better scalability than bus, but it too suffers from performance bottleneck since the hop count scales up with network size [11]. Figure A.1 illustrates a 4×4 2-D mesh architecture with wireless links.

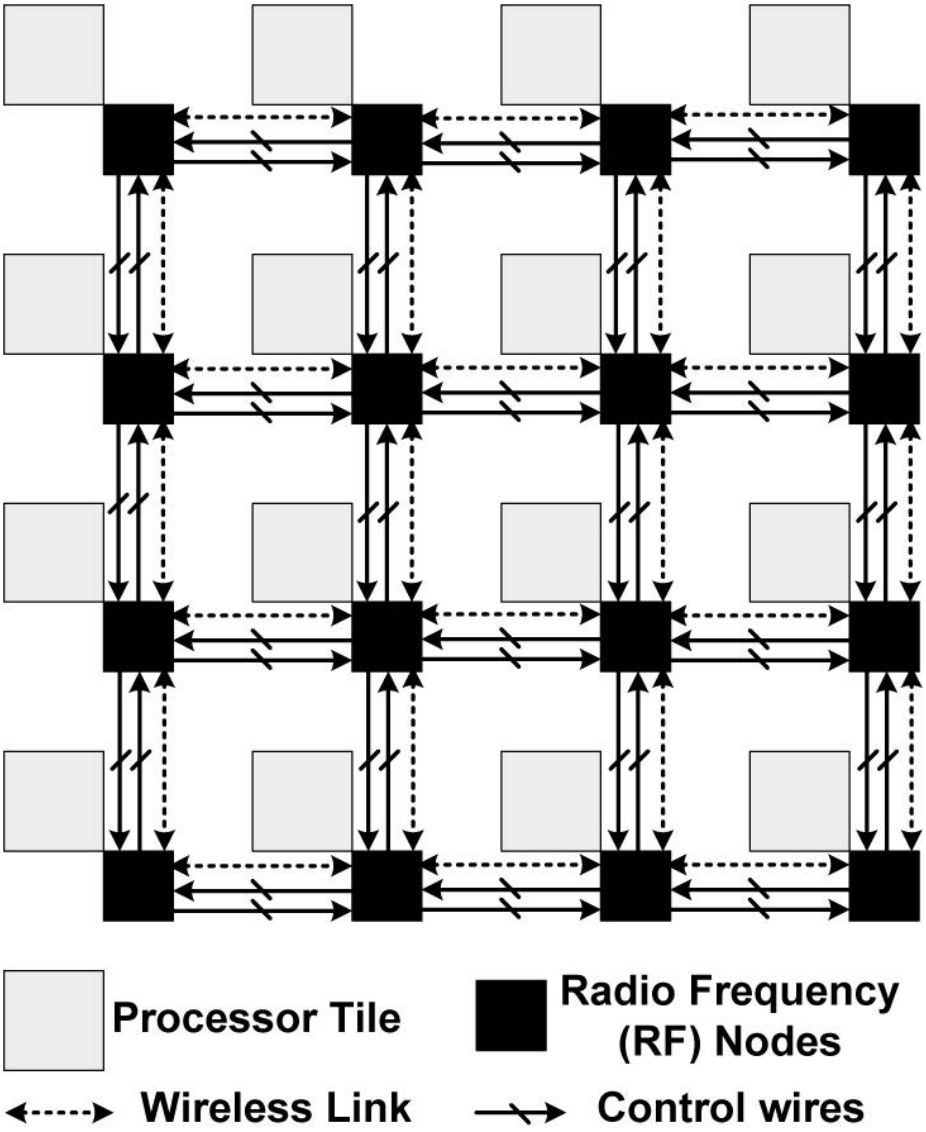


Figure A.1. 4 × 4 2-D mesh topology [104].

Appendix B
Quadratic and Linear Tapers

The tapers discussed in this Appendix can provide both impedance and field matching between CB-CPW and MS line types to realize a broadband transition.

B.1 Quadratic Taper

In quadratic taper, as illustrated in the Figure B.1, the width of the line w varies quadratically with position l along the length of the line as follows:

$$w = a_w l^2 + b_w l + c_w \qquad 0 \leq l \leq l_{tp} \tag{B.1}$$

where a_w, b_w and c_w are the unknown width coefficients to be determined. For CB-CPW lines, in addition to the width, the gap g can also be made to vary (independent of the width and) quadratically with position l as follows:

$$g = a_g l^2 + b_g l + c_g \qquad 0 \leq l \leq l_{tp} \tag{B.2}$$

where a_g, b_g and c_g are the unknown gap coefficients to be determined.

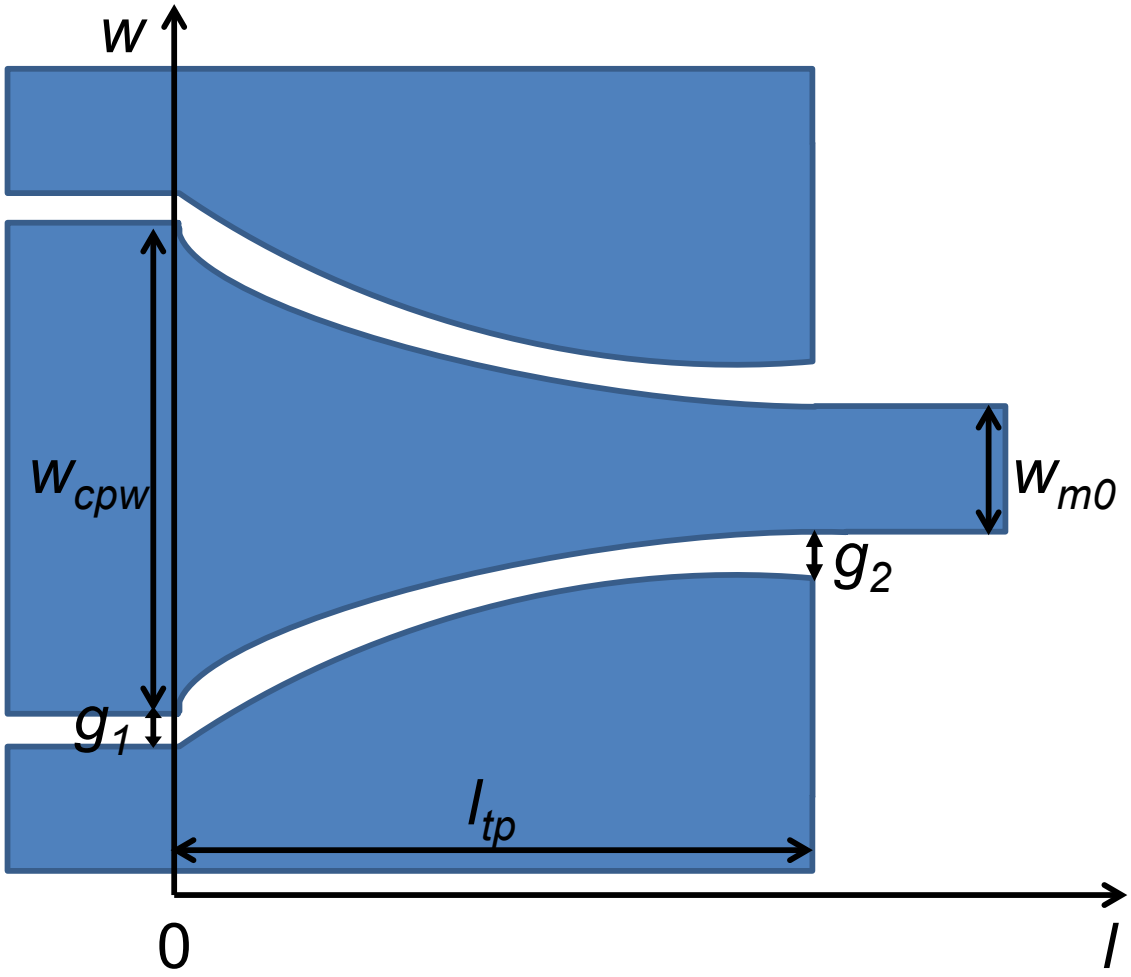


Figure B.1. Parabolic taper transition between CB-CPW and MS lines.

The coefficients can be found by applying the edge conditions and the user-defined curvature factor. For example, the width of the taper has to match the width of the CB-CPW and MS lines at the end points, as illustrated in Figure B.1. At $l = 0, w = w_{cpw}$ and from (B.1),

$$c_w = w_{cpw} \tag{B.3}$$

Substituting (B.3) in (B.1) gives

$$w = a_w l^2 + b_w l + w_{cpw} \tag{B.4}$$

At $l = l_{tp}, w = w_{m0}$ and from (B.4),

$$w_{m0} = a_w l_{tp}^2 + b_w l_{tp} + w_{cpw} \tag{B.5}$$

Let $w = d_w w_{m0}$ (where $d_w > 0$ is the width curvature factor) at $l = l_{tp}/2$ (taper midpoint). Then from (B.4),

$$d_w w_{m0} = a_w \frac{l_{tp}^2}{4} + b_w \frac{l_{tp}}{2} + w_{cpw} \tag{B.6}$$

Eliminating b_w from (B.5) and (B.6),

$$a_w = \frac{2[w_{m0}(1 - 2d_w) + w_{cpw}]}{l_{tp}^2} \tag{B.7}$$

Substituting (B.7) in (B.5),

$$b_w = \frac{w_{m0}(4d_w - 1) - 3w_{cpw}}{l_{tp}} \tag{B.8}$$

Substituting (B.7) and (B.8) in (B.4),

$$w = \frac{2[w_{m0}(1 - 2d_w) + w_{cpw}]}{l_{tp}^2} l^2 + \frac{w_{m0}(4d_w - 1) - 3w_{cpw}}{l_{tp}} l + w_{cpw} \qquad 0 \le l \le l_{tp} \tag{B.9}$$

Equation (B.2) can be solved similarly for gap g with a gap curvature factor $d_g = g/g_2$ defined at $l = l_{tp}/2$ (taper midpoint) and takes the following final form:

$$g = \frac{2[g_2(1 - 2d_g) + g_1]}{l_{tp}^2} l^2 + \frac{g_2(4d_g - 1) - 3g_1}{l_{tp}} l + g_1 \qquad 0 \le l \le l_{tp} \tag{B.10}$$

B.2 Linear Taper

A linear taper, as illustrated in Figure B.2, is just a specific case of the quadratic taper. For a linear taper, $a_w = 0$, which substituted in (B.7) gives

$$d_w = 0.5 + \frac{w_{cpw}}{2w_{m0}} \tag{B.11}$$

Substituting (B.11) in (B.8),

$$b_w = \frac{w_{m0} - w_{cpw}}{l_{tp}} \tag{B.12}$$

Substituting $a_w = 0$ and (B.12) in (B.4), the width w for linear taper varies as

$$w = \frac{w_{m0} - w_{cpw}}{l_{tp}} l + w_{cpw} \qquad 0 \leq l \leq l_{tp} \tag{B.13}$$

Following similar steps, the gap g for linear taper can be solved for and expressed as

$$g = \frac{g_2 - g_1}{l_{tp}} l + g_1 \qquad 0 \leq l \leq l_{tp} \tag{B.14}$$

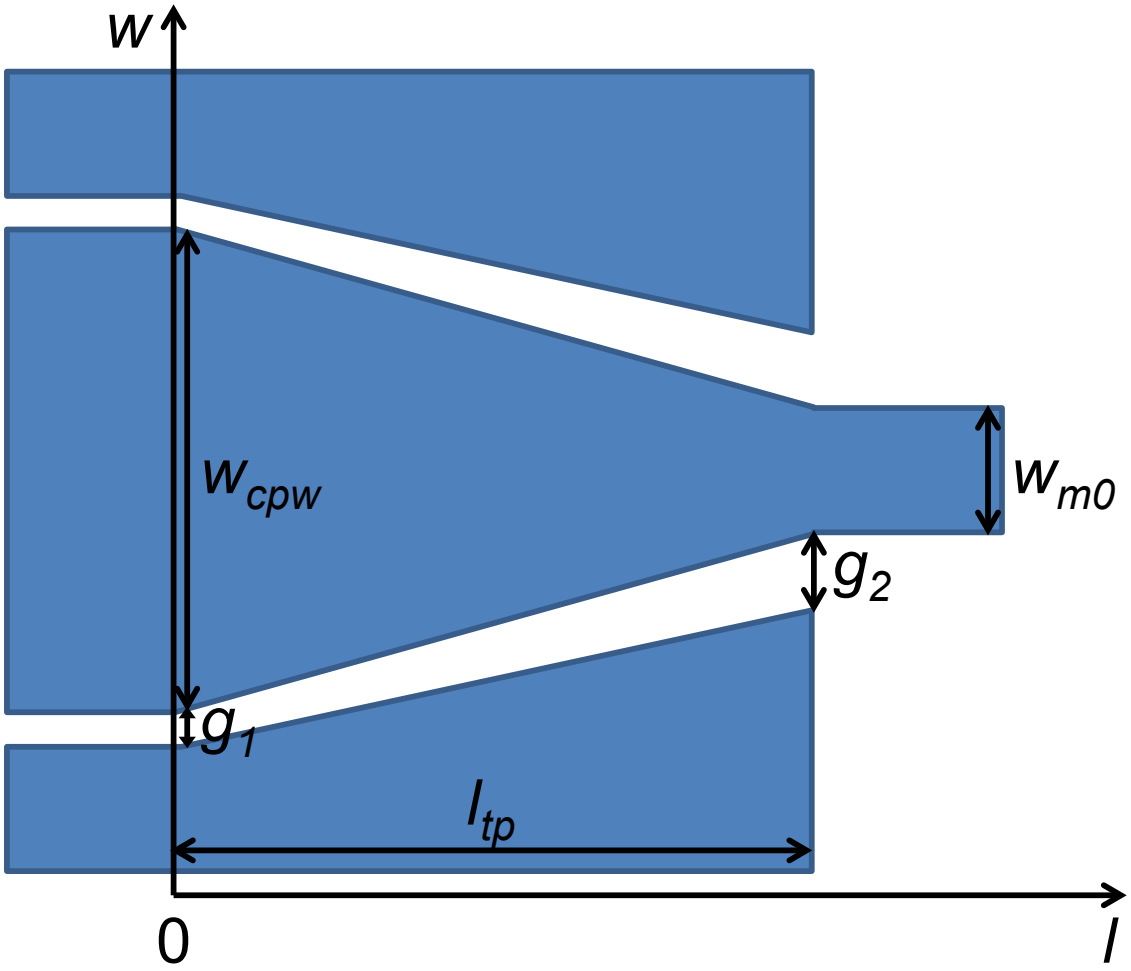


Figure B.2. Linear taper transition between CB-CPW and MS lines.

One interesting thing to note is that there is an optimal value for the gap g_2 (at the

CB-CPW/MS transition plane) to minimize the reflections. Initially, it is tempting to think that this gap should be as wide as possible so that the CB-CPW line at the transition plane looks more and more like the MS line causing the end reflection there to be reduced. However, a large g_2 causes the taper to be more abrupt increasing the intermediate reflections along the taper. It is the combined intermediate and end reflections that must be minimized to create a smooth taper, and not just the end reflection.

Appendix C
Calculation of Impedance for CB-CPW Tapers

Knowing the cross-sectional geometry of the CB-CPW line, as shown in Figure C.1, its characteristic impedance can be analytically calculated.

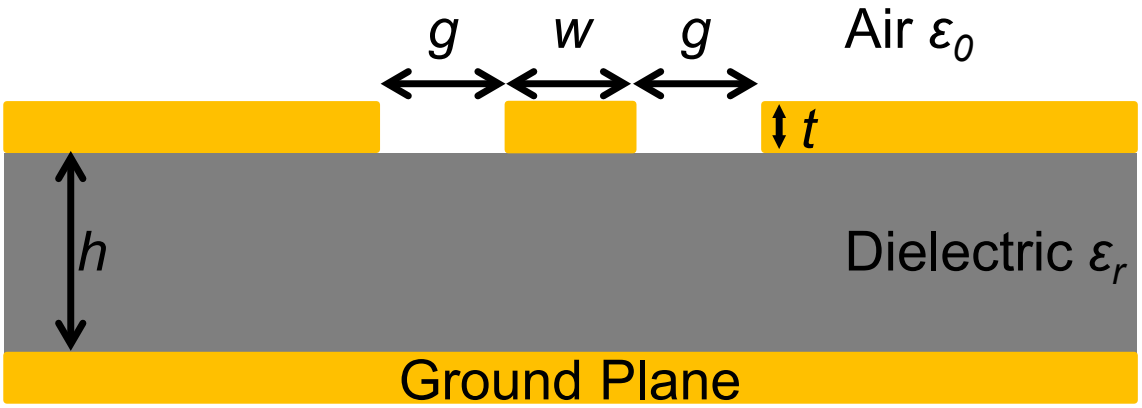


Figure C.1. Cross-section of CB-CPW line.

The formulas are derived assuming a quasi-TEM mode propagation on the structure with infinite bottom and side ground planes [81]. The effective relative permittivity $\epsilon_{r,eff}$ is first calculated as

$$\epsilon_{r,eff} = \frac{1 + \epsilon_r \frac{K(k')K(k_3)}{K(k)K(k_3')}}{1 + \frac{K(k')K(k_3)}{K(k)K(k_3')}} \tag{C.1}$$

where $K(k)$ is the complete elliptic integral of the first kind, and

$$k = \frac{a}{b} \tag{C.2a}$$

$$k_3 = \frac{\tanh(\frac{\pi a}{2h})}{\tanh(\frac{\pi b}{2h})} \tag{C.2b}$$

$$k' = \sqrt{1 - k^2} \tag{C.2c}$$

$$k_3' = \sqrt{1 - k_3^2} \tag{C.2d}$$

where a and b are related to the width w and gap g by

$$a = \frac{w}{2} \tag{C.3}$$

$$b = a + g \tag{C.4}$$

The characteristic impedance Z_0 of the CB-CPW line can then be calculated as

$$Z_0 = \frac{60\pi}{\sqrt{\epsilon_{r,eff}}} \frac{1}{\left[\frac{K(k)}{K(k')} + \frac{K(k_3)}{K(k_3')}\right]} \tag{C.5}$$

To take the finite conductor thickness t of the traces into account [81], the width w and the gap g are both corrected by adding the factor,

$$\Delta = 1.25t \frac{1 + \ln(\frac{2h}{t})}{\pi} \tag{C.6}$$

The corrected a and b are thus given by

$$a_c = a + 0.5\Delta \tag{C.7}$$

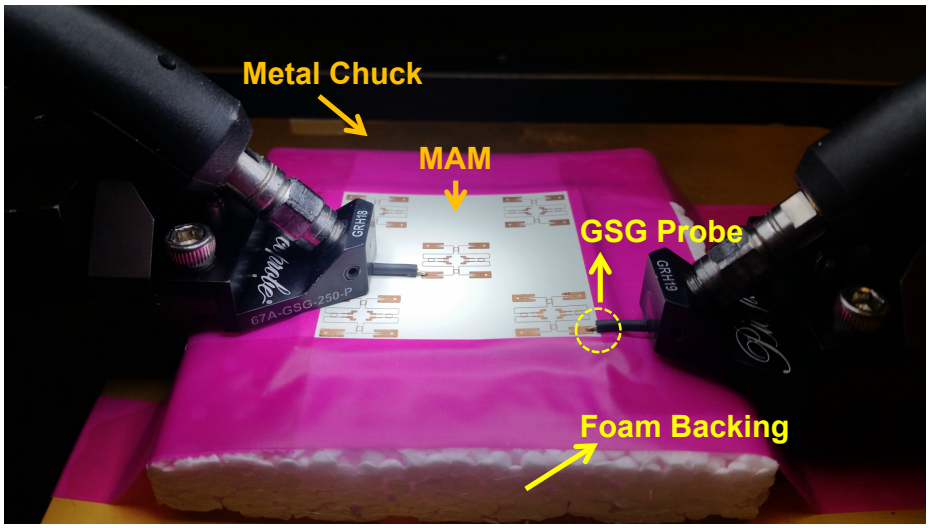
$$b_c = b + 1.5\Delta \tag{C.8}$$

which are used when calculating (C.2) and subsequently, Z_0 in (C.5). As w and g are varied when tapering, the Z_0 changes along the length of the taper.

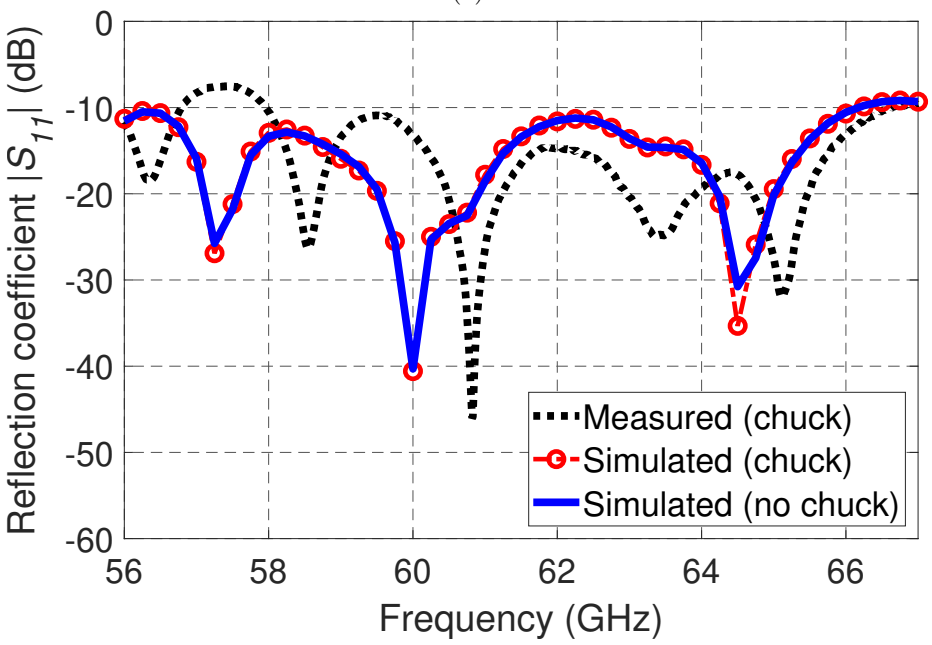
Appendix D

Measurement and Simulation in the Presence of the Metal Chuck

The fabricated MAM is placed with the antenna layer facing down on a foam backing of 12 mm thickness, as shown in Figure D.1(a). The foam backing itself is placed on the metal chuck. The foam is thick enough to avoid shorting of the antenna layer by the metal chuck underneath but still in the near-field of the antenna modules. The effect of the chuck is taken into account in the simulations by placing an infinite PEC plane 12 mm (i.e., the foam backing thickness) above the antenna layer. The fabricated prototypes are secured on the foam backing using tape when making the measurements, as shown in Figure D.1(a). This can also temporarily lessen bowing to some degree. The measured and simulated results are shown in Figures D.1(b) and D.2. When compared with the no chuck simulation results, one can see that the reflection coefficients are negligibly affected whereas the transmission coefficients are visibly perturbed by the presence of the chuck.



(a)



(b)

Figure D.1. (a) Measurement setup of the fabricated MAM prototype with foam backing and metal chuck underneath. (b) Reflection coefficient (dB) of an antenna module on the MAM with and without chuck.

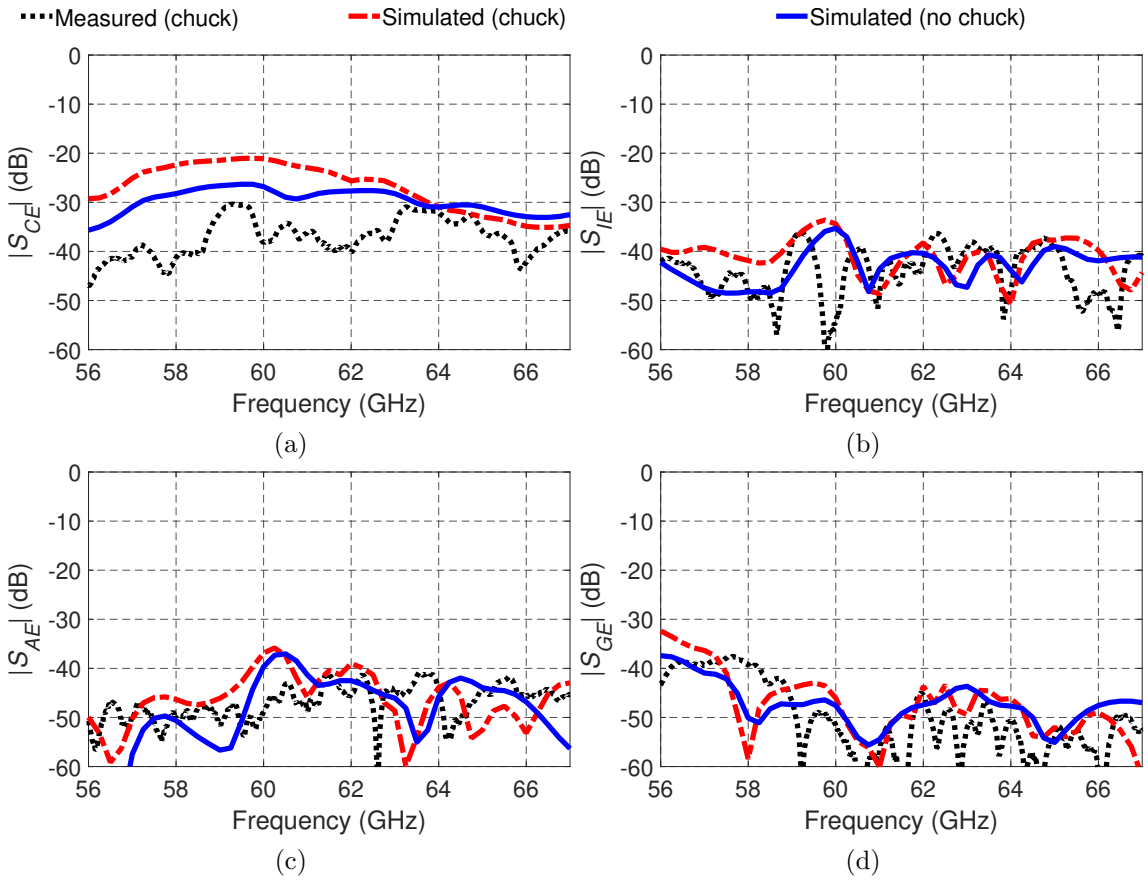


Figure D.2. Measured and simulated transmission coefficients (dB) between the antenna modules on the MAM with and without chuck. (a) $|S_{CE}|$. (b) $|S_{IE}|$. (c) $|S_{AE}|$. (d) $|S_{GE}|$.

Appendix E
Channel Capacity, Modulation Efficiency, SNIR, and BER

E.1 Channel Capacity

Shannon's theorem [106] provides the upper bound on the information carrying capacity C, in bits per second, of a channel given the channel's BW B_c and SNIR, expressed as

$$C = B_c \log_2(1 + \text{SNIR}) \tag{E.1}$$

SNIR is the ratio of average received signal power to average noise and interference power over the BW. From (E.1), it is easy to see that maximum possible bit rate depends on both B_c and SNIR. Moreover, SNIR can be traded for B_c and vice-versa. For example, the frequency modulation (FM) can outperform the amplitude modulation (AM) at lower SNIR but occupies more BW [107]. Increasing the BW, however, increases the noise power and degrades the SNIR. Therefore, trading off SNIR for BW can lower channel's capacity after some threshold value. Channel BW in the GHz range does not always translate to Gbps data rate. A channel with lots of noise and interference, for a given BW, is going to have lower capacity and higher BER [89]. The actual bit rate is usually much lower than the theoretical maximum given by the Shannon's theorem.

E.2 Modulation and Link Spectral Efficiency

Modulation type, and its particular hardware and software implementation, limit the achievable transmitted bit rate [25]. The performance of a modulation scheme is given by the modulation efficiency η_c, which is defined as the ratio of actual transmitted

bit rate R_c to the channel BW B_c, as follows:

$$\eta_c = \frac{R_c}{B_c} \tag{E.2}$$

Equation (E.1) only provides information about the SNIR required for achieving the capacity limit as the number of symbols $(M) \to \infty$ at an arbitrarily small BER. It does not specify at exactly what BER the limit is reached. The maximum achievable bit rate for a modulation scheme with finite M is further limited by Hartley's Law and it depends on the order $M = 2^{N_b}$ of the modulation, where $N_b = \log_2 M$ is the number of bits in a symbol [108]. Mathematically,

$$R_c \leq B_c N_b \tag{E.3}$$

M represents the number of distinct symbols (unique combination of bits) in a given modulation scheme. Higher order modulations, which have higher N_b, can increase η_c and R_c for a given BER but with higher SNIR requirement. Although increasing the SNIR increases the channel's capacity, it does not increase R_c for a particular modulation scheme used. It does, however, lower the BER [109]. Error-free communication can be achieved if data rate is sufficiently lowered. Nevertheless, it is desirable to allow for some error in data transmission in order to maintain high throughput. Extra bits, such as error-correcting codes (ECC) must be added in the bit stream to correct for errors when they do occur. Although ECCs add overhead to the bit stream, they can significantly improve a channel's data reliability. Use of ECC, however, decreases the useful data rate. Higher level network protocols add additional overhead that further reduces the data rate that is actually realized [25].

E.3 BER As a Function of SNIR

The SNIR is the ratio of average signal power S to the sum total of noise power N and interference noise power I, expressed as

$$\text{SNIR} = \frac{S}{N + I} \tag{E.4}$$

A channel with additive white gaussian noise (AWGN) is characterized by the noise power spectral density N_0 (W/Hz) [108] (e.g., background and thermal noise) and N is calculated as

$$N = N_0 B_c \tag{E.5}$$

Similarly, if the interference spectral density is known I_0, then

$$I = I_0 B_c \tag{E.6}$$

If the actual bit rate R_c is known, then the average energy per bit E_b can be calculated as [25]

$$E_b = \frac{S}{R_c} \tag{E.7}$$

Substituting (E.5), (E.6) and (E.7) in (E.4),

$$\text{SNIR} = \frac{E_b R_c}{(N_0 + I_0) B_c} \tag{E.8}$$

From (E.3), the maximum possible rate for finite M is $R_{c,max} = B_c N_b$ and the minimum SNIR required to achieve the rate $R_{c,max}$, from (E.8) simplifies to

$$\text{SNIR} = \frac{N_b E_b}{N_0 + I_0} = \frac{E_s}{N_0 + I_0} \tag{E.9}$$

where $E_s = N_b E_b$ is the average symbol energy.

The SNIR at the input of the RX detector determines the probability of a bit error (P_{r_b}), also called the BER. The detector cannot always correctly distinguish bits embedded in the signal due to the uncertainty caused by noise and interference. This results in the bit errors. Higher SNIR is desirable to reduce the uncertainty and BER. Given the SNIR, the BER for M-phase shift keying (M-PSK) and M-QAM modulation schemes can be calculated assuming gray mapping is used in the detector circuits [25]. The BERs are given by

$$P_{r_b}{}^{M-PSK} = \frac{2}{N_b} Q\left[\sqrt{2 N_b \frac{E_b}{N_0 + I_0}} \sin(\frac{\pi}{M})\right] \tag{E.10a}$$

$$P_{r_b}{}^{M-QAM} = \frac{4}{N_b}(1 - 2^{-\frac{N_b}{2}}) Q\left[\sqrt{\frac{3 N_b \frac{E_b}{N_0 + I_0}}{2^{N_b} - 1}}\right] \tag{E.10b}$$

where $Q[.]$ is the integral of the tail of the Gaussian density function. Using (E.10a) and (E.10b), the BER for a range of $E_b/(N_0+I_0)$ is plotted in Figure E.1. As $E_b/(N_0+I_0)$ increases, the channel becomes more robust to noise and the BER decreases. For a fixed $E_b/(N_0+I_0)$, the lower order modulation schemes have lower BER. The M-QAM scheme has lower BER than M-PSK scheme at any given $E_b/(N_0+I_0)$.

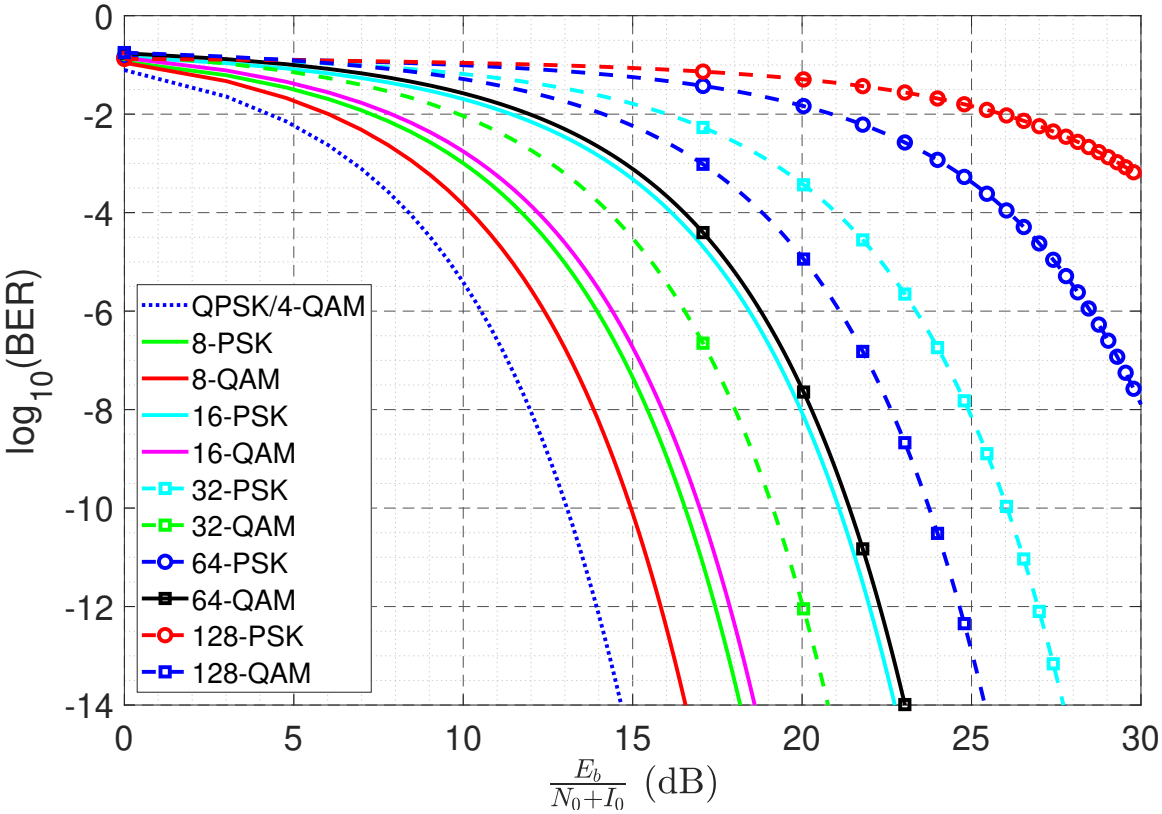


Figure E.1. Log probability of bit error as a function of $E_b/(N_0+I_0)$.

E.4 Channel Capacity and Modulation Efficiency As a Function of SNIR

If the actual transmission rate approaches the channel capacity i.e., $R_c \to C$, then (E.8) becomes

$$\text{SNIR} = \frac{E_b C}{(N_0+I_0)B_c} \tag{E.11}$$

Substituting (E.11) in (E.1), and rearranging,

$$\frac{E_b}{N_0 + I_0} = \frac{2^{\eta_{max}} - 1}{\eta_{max}} \tag{E.12}$$

where $\eta_{max} = C/B_c$ is the maximum possible spectral efficiency (Shannon's limit) in bits/s/Hz.

Equation (E.12) can be solved numerically for η_{max} [109] for a range of $E_b/(N_0 + I_0)$, as shown in Figure E.2. The increase in $E_b/(N_0 + I_0)$ is accompanied by the increase in the channel capacity C and η_{max}.

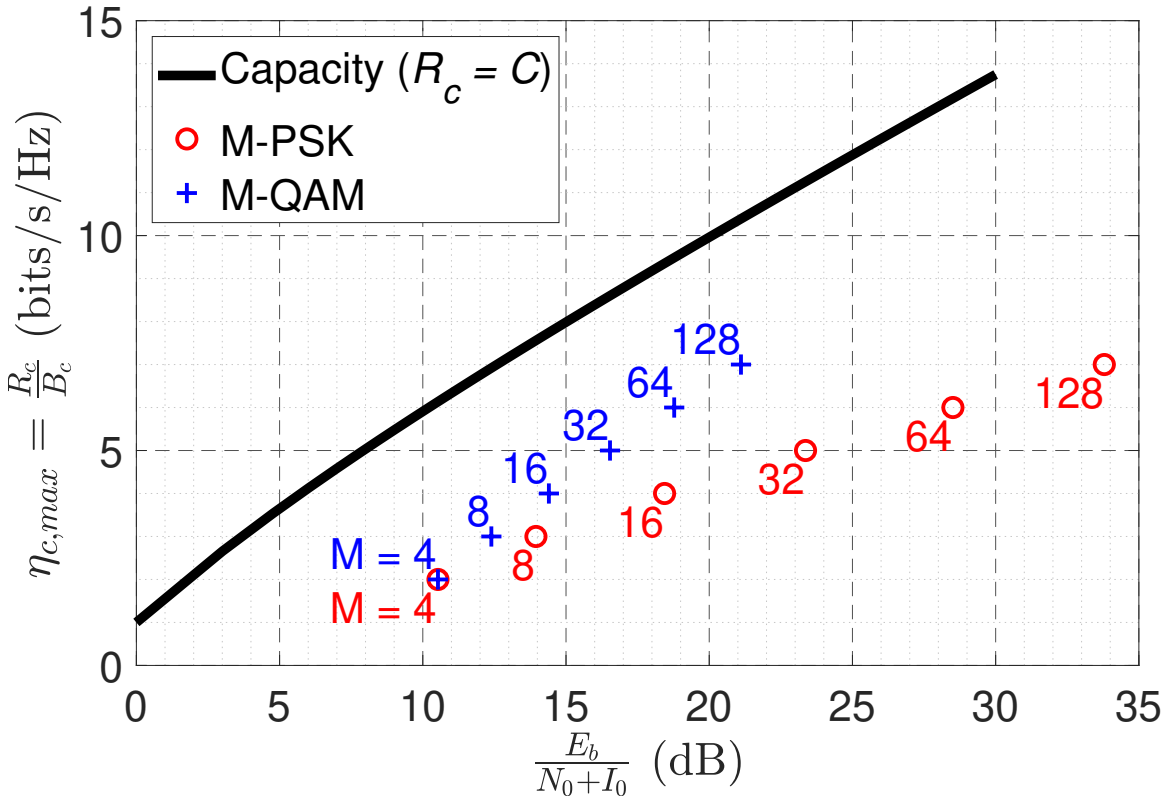


Figure E.2. Maximum modulation efficiency comparison of M-PSK and M-QAM modulation schemes at BER = 10^{-6}.

In practice, a modulation scheme with finite M has to be used and therefore, from (E.2) and (E.3), the maximum modulation efficiency $\eta_{c,max}$ in bits/s/Hz is limited to

$$\eta_{c,max} = \frac{R_c}{B_c} = N_b \tag{E.13}$$

where $\eta_{c,max} < \eta_{max}$.

The $E_b/(N_0 + I_0)$ required to achieve $\eta_{c,max}$ for a given BER can be obtained by numerically solving (E.10a) and (E.10b) for M-PSK and M-QAM schemes, respectively. This is done in MATLAB for M = 4, 8, 16, 32, 64, and 128 at BER = 10^{-6} for M-PSK and M-QAM and the results are shown in Figure E.2. The higher order modulation schemes have higher $\eta_{c,max}$ at the given BER but they also require higher $E_b/(N_0+I_0)$ to achieve the higher data rate. From Figure E.2, it can be seen that the M-QAM scheme requires lower $E_b/(N_0 + I_0)$ than the M-PSK scheme to achieve the same throughput at the same BER. Once $E_b/(N_0 + I_0)$ is known, the SNIR required can be found from (E.9).

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